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THE DYNAMIC RANGE OF TIMING MEASUREMENTS OF THE ASYNCHRONOUS SIGMA-DELTA MODULATOR

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Abstract: The mapping of the signal amplitude into the timing sequence using the asynchronous Sigma-Delta modulation is investigated in the paper. Input signal reconstruction according to Lazar-Tóth theorem is assumed. The analysis presented in the paper shows that the utilization factor η is the main input parameter determining the speed of the modulator operation, and the range of output timing measurements. The fundamental tradeoffs of the asynchronous Σ-Δ modulator design for signal conversion are discussed. *Copyright © 2006 IFAC*

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1. INTRODUCTION

Although today's commercial digital circuits are almost exclusively synchronized using the global clock, the asynchronous circuits and systems, which were introduced in the early 50s, receive now increasing interest due to its promise of more efficient design. Supporting clocks comes at very high engineering costs, especially in the context of the trend towards deep submicron VLSI technology. One of the increasingly important issues is clocking power due to the packaging and cooling issues that highly dissipative circuits involve.

The nature of the asynchronous circuits allows them to remain in a stable state until necessary transitions trigger an event of interest. This avoids synchronizing the events using a global clock tree that can consume a large amount of energy. Eliminating the global clock, which synchronizes all parts of circuit in synchronous logic, provides more flexibility to design system architectures. The well-known benefits of the asynchronous circuits are speed, low energy dissipation, modular design, immunity to metastable behavior, freedom from clock skew, and low generation of and low susceptibility of electromagnetic interference.

Undoubtedly, the strong point of the synchronous systems is the well-established system theory, design and analysis. At the same time, the theory of the asynchronous approach seems to be still in its infancy.

The development of new asynchronous design methodologies requires supporting background research on the several aspects of the asynchronous functionality. The implementation of the fully asynchronous architecture demands the complete revision of the whole signal processing chain, since the time is no longer an independent variable in system modelling and design.

One of principal problems of the clock-less architecture is the issue how to acquire the information from the environment on the input of the system. The natural sampling strategies for asynchronous circuits are *signal-dependent*, rather than *time-triggered*.

In the signal-dependent sampling, the system input is fed by signal amplitude variations so the sampling occurs "when it is required". Consequently, the

temporal density of sampling operations varies in the time, and is determined by input signal changes.

The most common signal-dependent sampling strategy is the *level-crossing scheme*, where the sampling is triggered if the input signal crosses prespecified levels disposed along the amplitude domain. The analysis of the mean sampling rate in the level-crossing scheme is presented in (Miśkowicz, 2004). Some extensions of the level-crossing scheme have been also proposed, e.g. *integral sampling* (Miśkowicz, 2005a), or *sampling in energy domain* (Miśkowicz, 2005b).

The time becomes a *dependent variable* in signal-dependent schemes. The temporal properties of the discrete sequence are determined by the value assumed to be an independent variable, which is directly (in the level-crossing sampling) or indirectly (e.g. in the sampling in energy domain) the signal amplitude.

Thus, in order to record the digital representations of the continuous-time signal, we have to turn over the amplitude axis to the time axis and to quantize the latter rather than the former. The idea of *time-to-code converters* (Kirianaki *et al.*, 2002) becomes a significant alternative for signal processing in sensory instrumentation.

In this paper we follow the idea presented by Lazar and Tóth (2004), which relies on mapping the signal amplitude information into the timing sequence using the asynchronous Sigma-Delta (Σ-Δ) modulation. The temporal properties of the waveform on the output of the asynchronous Sigma-Delta (Σ-Δ) modulator are investigated.

Our contribution is the formulation of the fundamental tradeoffs of the asynchronous Σ-Δ modulator design. In particular, we show that the utilization factor is the main input parameter determining the speed of modulator operation, and the range of output timing measurements. We evaluate the bounds of time interval lengths that have to be encoded in order to recover the original bandlimited continuous-time signal. The presented analysis is a preliminary work in the development of the asynchronous analog-to-digital conversion methodology.

2. PRINCIPLES OF ASYNCHRONOUS Σ-Δ MODULATION

The asynchronous Sigma-Delta (Σ-Δ) modulator is simple, does not require any clocking, matches well with CMOS technology and can operate at low current and supply voltage. The modulator consists of the lowpass filter (integrator), and the non-inverting Schmitt trigger operating in a negative feedback loop (Fig. 1).

The idea of the asynchronous Σ-Δ modulation was formulated in the 60s (Das and Sharma, 1967). However, to the recent time when Roza, (1997), and Lazar and Tóth (2004) published their significant papers, the use of the asynchronous Σ-Δ modulation for signal conversion has been of little interest to scientific and engineering community.

2.1 Asynchronous Σ-Δ Operation.

The principle of the asynchronous Σ-Δ modulator operation is that the difference between the input $x(t)$ and the output $z(t)$ signals is integrated until one of Schmitt trigger thresholds $\{-\delta,\delta\}$ is reached. Then, the output of the trigger is reversed, and the integration starts again. The waveforms on the integrator output $y(t)$, and the Schmitt trigger output $z(t)$ for the DC level input signal are shown in Fig. 2.

In order to ensure that the signal $y(t)$ on the integrator output is a monotone increasing or decreasing function of the time, the maximum absolute input signal value c should be smaller than the Schmitt trigger output b, that is, $|x(t)| \le c < b, t \in R$.

Assume that the Schmitt trigger has symmetrical thresholds $\{-\delta,\delta\}$. The output of the Schmitt trigger might stay at one of $\{-b,b\}$ states. If the Schmitt trigger is in the state $\{b,\delta\}$ at a certain instant, then due to the negative feedback the input to the Schmitt trigger $y(t)$ decreases in the time to its maximum negative value $-\delta$. When the value $-\delta$ is reached, the trigger output reverses to $-b$. Then, the signal $y(t)$ starts to grow from $-\delta$ to δ. When the maximum value δ is reached, a transition of the output from $-b$ to b is released.

Thus, the square wave $z(t)$ on the output of the Σ-Δ modulation has a constant amplitude, but its transition times are nonuniformly spaced. The lengths of time intervals between consecutive transitions depend on the input signal behavior. We treat the length of a particular time interval as a *sample*, since it carries the information about the input signal amplitude. Due to the integration, the sampling scheme belongs to the *signal-dependent integral sampling* (see (Miśkowicz, 2005a) for the analysis of the other integral sampling algorithm).

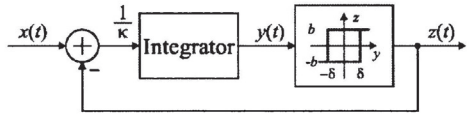

Fig. 1. Asynchronous Sigma-Delta (Σ-Δ) modulator.

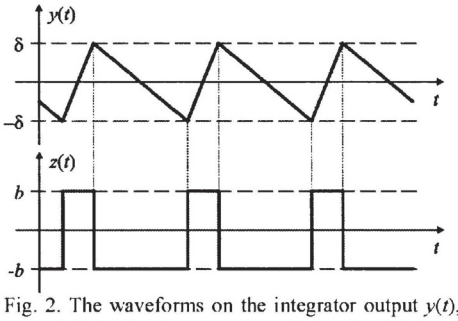

Fig. 2. The waveforms on the integrator output $y(t)$, and Schmitt trigger output $z(t)$ for the DC level input signal: $x(t) = d \le c < b, d = \text{const}, t \in R$.