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Research article

Redundant and fault-tolerant algorithms for real-time measurement and control systems for weapon equipment

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ABSTRACT

Because of the high availability requirements from weapon equipment, an in-depth study has been conducted on the real-time fault-tolerance of the widely applied Compact PCI (CPCI) bus measurement and control system. A redundancy design method that uses heartbeat detection to connect the primary and alternate devices has been developed. To address the low successful execution rate and relatively large waste of time slices in the primary version of the task software, an improved algorithm for real-time fault-tolerant scheduling is proposed based on the Basic Checking available time Elimination idle time (BCE) algorithm, applying a single-neuron self-adaptive proportion sum differential (PSD) controller. The experimental validation results indicate that this system has excellent redundancy and fault-tolerance, and the newly developed method can effectively improve the system availability.

1. Introduction

Modern warfare has put increased requirements on weapon availability. As multiple functions like high-speed data bus interface, control and self-testing were integrated into the on-board weapon equipment, problems such as various kinds of interfaces and increased test data information amount were brought about. To this end, measurements of equipment and control systems have gained increased importance [1]. Real-time systems in critical areas must ensure their real-time properties, and additionally ensure that the tasks can be correctly accomplished on time even in system failures. Hence, a real-time system must have some fault-tolerance capability. The present methods of achieving hardware fault-tolerance are mainly by constructing a redundant system. For example, Xu and Liu et al. [2] from the Harbin Institute of Technology, China, proposed a "3+1" hybrid redundant structure of three-module redundancy with a single hot-swap module to improve the fault-tolerance of the system. A three-module redundancy management card was designed to provide the embedded system with the key functions of decision, reconstruction and hot backup. For a hot-redundant system, a good hot-swap technique is the key to ensure quality and flexibility. Yi Chen and David Ki-Wai Cheng, from Hong Kong Polytechnic University, proposed a simple hot-swap solution for parallel power modules that uses current-sharing (CS) interface circuits [3]. This hot-swap of power modules was achieved for high-availability parallel power module systems.

Software fault-tolerance [4] can be achieved by re-executing a task that has experienced a fault or by executing its backup task. A fault-tolerant real-time scheduling algorithm effectively combines software fault-tolerance with the real-time scheduling algorithm of a real-time system to ensure the fault-tolerance and availability of the system. Optimal scheduling here means to produce a correct schedule whenever possible. In real-time embedded systems, tasks must be completed by specified deadlines. When task deadlines are equal to their inter-release times, this problem can be solved by scheduling approaches, where the scheduler manages a global task queue, and tasks can migrate from one processor to another, e.g., Bonifaci and Brandenburg [5], Biondi et al. [6], Guasque et al. [7], Massa et al. [8], Easwaran et al. [9], Funaoka et al. [10], Funk [11], and Levin et al. [12]. Unfortunately, most approaches incur an excessive overhead of preemptions and migrations by subdividing and over constraining all tasks to run within small time intervals. During recent decades, many studies have been conducted on the problem, and a host of algorithms have been proposed [13–15], among which the two most-studied real-time scheduling schemes are the Rate Monotonic (RM) scheduler and the Earliest Deadline First (EDF) scheduler [15]. Beitollahi [16] studied how to add appropriate and efficient time redundancy to the Earliest-Deadline-First (EDF) algorithm for periodic real-time tasks. Based on reserving sufficient slack, Ghosh [17] proposed two algorithms, the FSP (feasible shortest path) and LTH (linear time heuristic) algorithms, to solve the problem of

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adding fault-tolerance to a queue of real-time tasks. Bertossi established two versions, a primary and an alternate, for each task [18]. The fault-tolerant model of primary/alternate versions has been widely applied and studied in real-time scheduling [19–21]. In order to execute the primary version as often as possible, Ding W et al. proposed the off-line backwards-RM scheme to pre-allocate time intervals to the alternate version and the on-line RM scheme to dispatch the primary version [22]. To reduce the dynamic scheduling expense of setting aside time to run an alternate version, Han et al. proposed the BCE algorithm [23]. This algorithm achieves good scheduling performance when processor utilization is low. However, when it is high, it has a high loss rate of the primary task because it cannot use the Checking Available Time (CAT) algorithm to obtain a good executable prediction of the primary task.

2. Overall design of the system

In this paper, we present improvements that have been designed for the Compact PCI (CPCI) bus measurement and control system. This bus system is currently widely used in measurement and control systems for weapon equipment. Our improvements include hot redundant fault-tolerant performance from the aspects of both hardware and software. First, our work improves the CPCI bus device and the structural composition of the system. We use the hot-swap technique in a high-availability mode and hence establish a redundant fault-tolerant system. Second, for the challenge of achieving fault-tolerance for the highly real-time CPCI measurement and control system, we enhance the original classical BCE algorithm with a new designed BCE-Update algorithm and a PSD-BCE-Update algorithm that achieve a higher fault-tolerance for a real-time system.

Fig. 1 is the architecture of the whole measurement and control system. It is composed of an upper computer, a lower computer

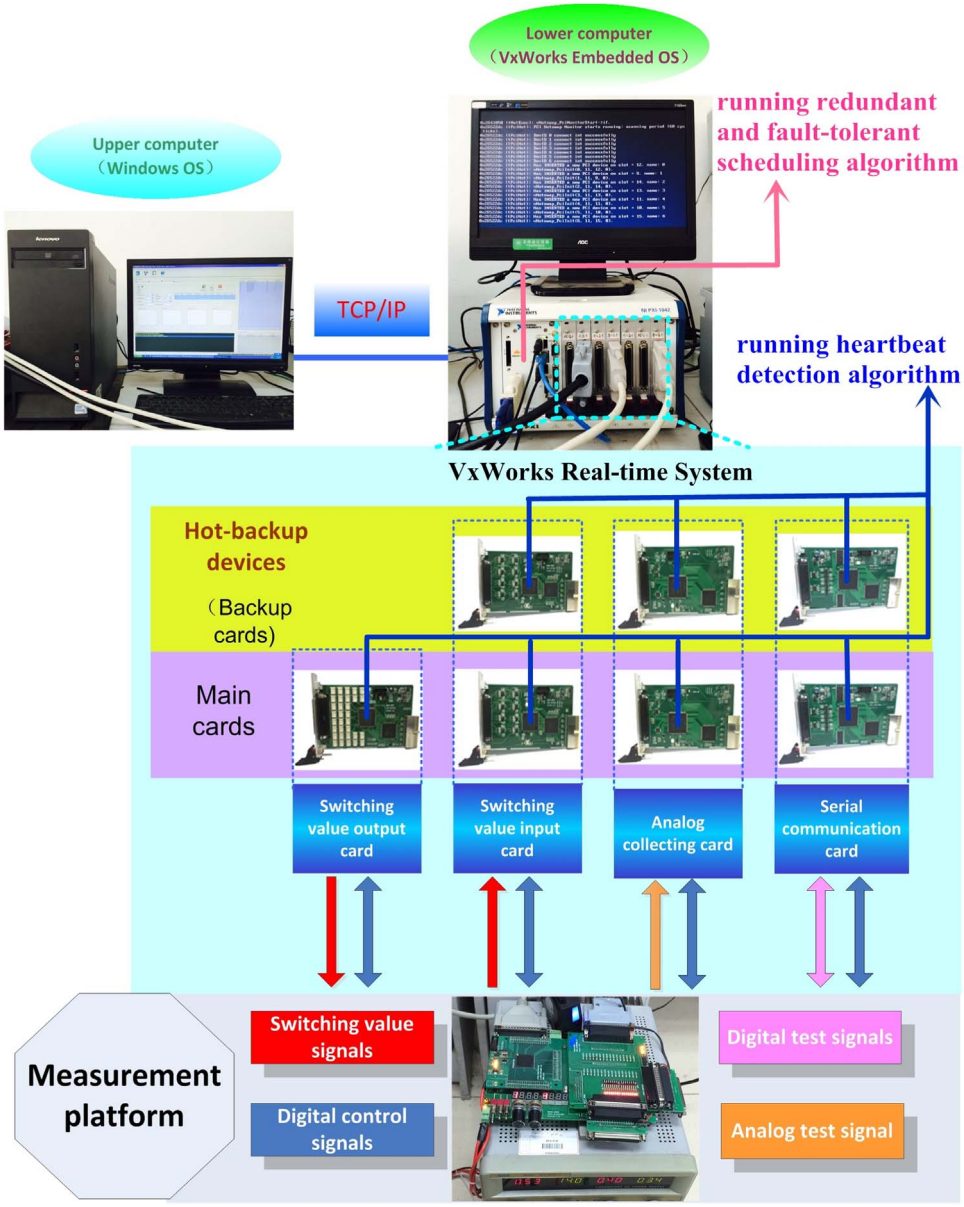

Fig. 1. System architecture.

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