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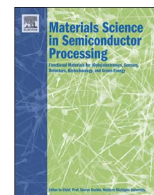

Impact of thin high-k dielectrics and gate metals on RF characteristics of 3D double gate junctionless transistor

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ABSTRACT

RF performance of 3D double gate junctionless transistor (JLT) is investigated considering thin high-k dielectrics and gate metals. The 3D double gate junctionless transistor (JLT) with 20 nm gate length is designed and simulated in order to study the RF parameters such as transconductance, transconductance generation factor, output conductance and resistance, intrinsic capacitance, cut-off frequency, early voltage, and intrinsic gain. High-k dielectric gate oxide and gate metals have effect on the DC characteristics of JLT. However, in order to evaluate the impact of high-k gate dielectrics on the RF performance of the device, SiO_2, Si_3N_4, HfO_2 dielectrics are considered and compared their performances. Furthermore, the effect of various gate metals on RF performances of the device is also discussed. Gate oxide with higher-k value improves the transconductance, output conductance, and intrinsic gain of the device. While, gate metal with lower work function exhibits better RF characteristics in JLT, application of different high-k dielectrics and gate metal have no improvement in cut-off frequency. The investigation gives an idea to optimize the RF performance of the device using suitable gate dielectric and gate metal. This investigation helps to create an opportunity for the junctionless transistor to realize high performances RF circuits.

1. Introduction

Presently, transistor scaling has reached to 22 nm node and expected to reach beyond 10 nm by 2026 [1]. In the process of miniaturization, MOS devices are facing various challenges in nanometre regime. Down scaling of device weakens gate control and gives rise to short channel effects like drain induced barrier lowering (DIBL), threshold voltage roll-off, hot carrier effect and poor subthreshold swing. These constrains are responsible for performance degradation in the MOS devices [2,3]. Arduous search for improvement in gate control leads to explore new semiconductor devices. Along with technology improvement, various methodologies like channel engineering, gate engineering, silicon on insulator, multi-gates and gate stack are tried to overcome the short channel effects. Multi-gate structures have helped to improve the gate control to an extent in suppressing the SCEs [4–8]. Though double-gate and FINFET structures of MOSFET have shown immense improvement to control SCEs, inversion mode devices require very shallow junction for down scaled design. Requirement of abrupt junctions and non-uniform channel doping increased the process complexity and restricted nano-manufacturing.

Junctionless Field Effect Transistor (JLFET) was proposed as a solution to the problems faced by inversion mode FETs [9,10]. As it is a uniformly doped device, it gives an ease of fabrication. Moreover, JLTs have no junction and act like a gated resistor [11,12]. Unlike inversion mode (IM) MOSFET, JLT conducts in bulk and full depletion of channel is compulsory to turn off the device. So double gate structure is undoubtedly useful to ensure full depletion. Because of interesting characteristics of JLT, simulations and analytical models were done to understand the fundamental of the same [13–16]. Furthermore, the device has shown good characteristics for high temperature and drain current increases with temperature [17]. Several attempts were made to demonstrate the viability of the device performance for circuits, like: inverter, pass transistor, SRAM, resonator and CMOS logic gates etc. [18–22].

Though junctionless accumulation mode transistor was reported as inferior to IM transistor [23], heavily doped junctionless multi-gate structure shows reduced SCEs compared to inversion-mode MOSFETs [24]. Due to low parasitic capacitance and high transconductance in JLT, we get an improved analog performance [25]. Due to low on current, JLT shows poor cut-off frequency and energy-delay product compared to IM MOSFETs [21]. To increase the on-current, high-k dielectric is used for gate oxide and dc characteristics were investigated

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for different dielectric and different gate metals [26]. Thereafter, performance of JLT based inverter with different high-k dielectrics was investigated and it was observed that high-k gate dielectric improves circuit performance [22]. The key analog figure of merits (FOMs) like transconductance generation factor (TGF), intrinsic gain (A_V) and cut-off frequency (f_t) are degraded due to SCEs. Changes in gate oxide and gate material can have an impact on these FOMs. In order to give a full understanding of the device and for both low and high power applications, we require proper investigation of analog/RF characteristics.

We propose to present the insights of ac characteristics of the 20 nm double gate junctionless transistor. Furthermore, we have investigated the effects of different gate dielectrics and different gate metal on its analog characteristics. A systematic investigation on device characteristics like transconductance (g_m), drain conductance (g_D) and resistance (R_O), transconductance generation factor (TGF), intrinsic gain (A_V), gate capacitance (C_{gg}) and cut-off frequency (f_t) is performed using 3D TCAD simulation. After the introduction, Section 2 describes the junctionless transistor structure dimensions, its material and doping concentrations. Section 3 describes the simulation environment of 3D Synopsis TCAD. This section also analyses the physics models and methods used in simulation model. Investigation results and analysis are given in Section 4 and finally concluded in Section 5.

2. Device structure and parameters

As shown in Fig. 1, we have considered a double gate JLT with 20 nm gate length [26] for our investigation. Channel thickness of 10 nm is used to ensure full depletion at off condition and the channel is doped (1.5×10^{19} cm^{-3}) with Arsenic. To increase the gate control over channel, we have used different high-k gate material for investigation. Moreover, different other structures are also designed with different gate materials. All the device structure dimension and parameter related details are furnished in Table 1. In our study, we have used specific parameter values like work function and dielectric constant for our simulated devices. These parameter details are given in Table 2.

3. Simulation method

We have used commercially available Synopsys TCAD tools to develop and optimize our devices. Total simulation can be divided in three parts: device structure preparation, device physics simulation and data extraction. JLT structures are prepared using Synopsys 3D device structure editor, physics is simulated by Synopsys Device Simulator (Sdevice) and output plotting and data extractions are performed using Svisual, Inspect and Origin. Synopsys 3D device structure editor helps to prepare different device in an interactive way and massing engine is called using interface. Sdevice simulates the devices for specific conditions with the help of advance physical models and robust numerical methods. Separate parameter files are included in Sdevice simulator to mention the specific values of the parameters mentioned in Table 2.

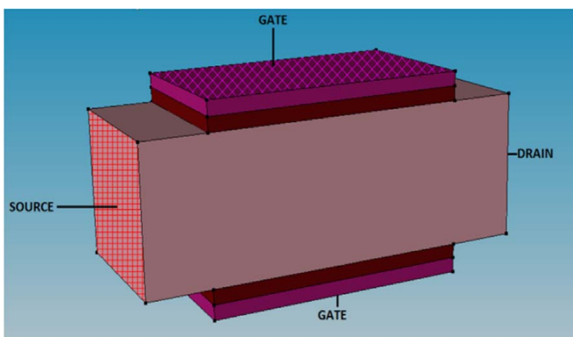

Fig. 1. 3D structure of double gate junctionless transistor.

Table 1
Device parameters of the junctionless transistor.

Parameters	Values
Gate Length (L_g)	20 nm
Gate Width (W)	12 nm
Channel Thickness (T_{si})	10 nm
Doping of the channel (N_D)	1.5×10^{19} cm^{-3}
Donor	Arsenic
Front Gate Oxide Thickness (T_{oxf})	1 nm
Back Gate Oxide Thickness (T_{oxb})	1 nm
Gate oxide type	SiO_2, Si_3N_4, HfO_2
Gate metal type	Al, Poly-Si, Ti, Au

Table 2
Metal work function and oxide dielectric constant used in of the junctionless transistor.

Materials	Dielectric constant (K)	Work function (eV)
SiO_2	3.9	–
Si_3N_4	7.5	–
HfO_2	25	–
Al	–	4.28
Ti	–	4.33
Poly-Si	–	4.4
Au	–	5.1

Different models like drift-diffusion model for current transport, High Field Saturation model for mobility, mobility degradation model Enormal, recombination models of Auger, SRH and avalanche are included for the device physics simulation. For verification of the simulation results, the simulator model parameters are calibrated with an experimental data available for junctionless transistor [27] as shown in Fig. 2. The simulator so calibrated is used for our study.

In this study, high-k dielectrics are used in place of SiO_2 to investigate its effect on RF performance of the device. As the cause of mobility degradation by high-k dielectric is not well understood, there is no specific fixed model for it. Instead of using single doping dependent mobility model, several mobility degradation models are used to estimate the mobility degradation. Enhanced Lambordi model with high-k dielectric, remote phonon scattering model and remote columb scattering models are incorporated with Masetti model. These interface specific models are used for high-k interfaces. Furthermore, recombination models for general interface are also included, along with trap charges to realize the practical effects on the device performance. Trap charges are dependent on the deposition process chosen in the fabrication process [28]. As SiO_2 has positive charges at silicon interface and HfO_2 and Si_3N_4 have negative charges for their interface with silicon, we have included it in the simulation process. Negative charges

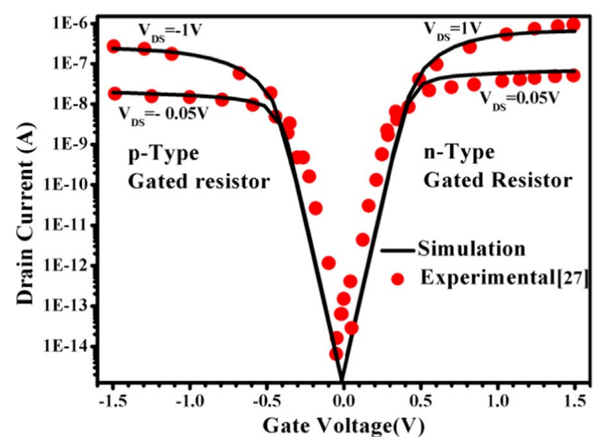

Fig. 2. Calibration against the experimental data of drain current of n-type and p-type gated resistor (JLT) for 1μmgate length and 30 nm width [27].

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