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Fully coherent Ge islands growth on Si nano-pillars by selective epitaxy

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ABSTRACT

Our recent experimental results of Ge nanoheteroepitaxy (NHE) on Si nanopillars (NPs) are reviewed to confirm the possibility of relaxed Ge growth on Si without misfit dislocations (MDs) formation by elastic deformation. Selective Ge growth is performed by using reduced pressure chemical vapor deposition (CVD) on two types of Si NPs with thermal SiO_2 or CVD SiO_2 sidewalls and on Si nanoislands (NIs) on SiO_2. By using thermal SiO_2 sidewall, compressive strain is generated in the Si pillar and fixed by the thermal SiO_2. This results in an incoherent Ge growth on Si NPs due to MD formation. By using CVD SiO_2 sidewall, tensile strain formation due to thermal expansion during prebake for Ge epi process is observed. However, strain in Si due to Ge growth is not dominant. By introducing a $Si_{0.5}Ge_{0.5}$ buffer layer, no MD and stacking faults are observed by cross section TEM. The shape of Ge on Si NPs becomes more uniform due to improved crystal quality. On Si NIs on SiO_2, a clear compliance effect is observed after Ge growth. Coherent growth of Ge on Si is also realized on Si NIs by using $Si_{0.5}Ge_{0.5}$ buffer.

1. Introduction

Alternative material integration into silicon (Si) based semiconductor technologies is of increasing interest, since the requirements of future electrical devices become more and more complex e.g. for ultra-broadband telecommunication, image sensing etc. However, downsizing of scaling to improve device performance is getting close to the limit due to material properties of Si. Therefore in order to extend the device performance further, integration of more functions like optoelectronic devices into complementary metal oxide semiconductor (CMOS) technology, is widely investigated [1–3]. For optoelectronic device integration, Germanium (Ge) heteroepitaxial growth is especially interesting because of its compatibility to Si based processes [4]. However, 4.2% lattice mismatch causes crystal quality degradation due to misfit dislocations (MDs) and threading dislocations (TDs) (Fig. 1a). Due to the high lattice mismatch between Ge and Si the critical thickness of a Ge layer on Si is limited to the range of several nm only. Therefore, it leads to a high density of misfit dislocation at the interface between Si and Ge and TDs in the deposited Ge layer. The TDs in Ge degenerate the electrical properties (e.g. increase of dark current for optoelectronics applications) [5]. In order to improve the TD density in Ge, one way is to introduce a thick graded SiGe buffer layer. By depositing a graded SiGe buffer, the lattice mismatch between Si and Ge can be introduced gradually, resulting in a three-dimensional misfit dislocation network and TDs are generated in the graded SiGe buffer [6]. But during the graded SiGe buffer growth, the surface roughness is also enhanced. Another approach to deposit high crystal quality Ge is a direct Ge deposition with annealing to move dislocation networks. Thermal cycling processes [7] after Ge deposition, and cyclic annealing, which is an annealing process interrupting the Ge growth [8] followed by vapor phase etching [9], are reported. Another possible approach for high quality Ge growth is thick selective Ge epitaxy in high aspect ratio window [10]. Using this technique, dislocations will be terminated at the sidewalls of the aspect ratio window, because dislocations runs in {111} plane. As a result, the upper part of the selectively grown Ge becomes dislocation-free. The aspect ratio trapping technique is also demonstrated in lateral direction for high quality local GeOI fabrication [11]. Selective Ge growth on Si micropillar [12] is another technique to deposit dislocation-free Ge. The relaxation mechanisms shown here are MD formation near interface between Si

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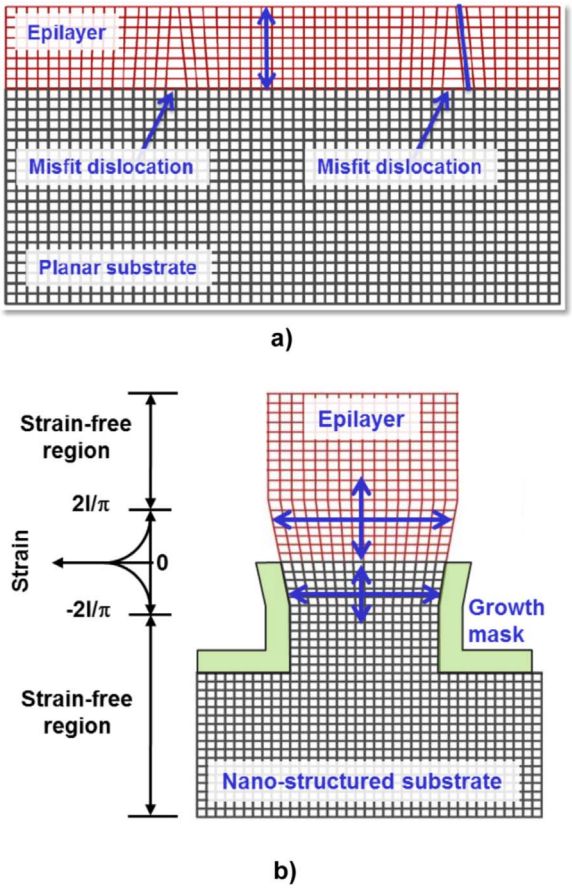

Fig. 1. Schematic diagram of (a) planar Ge layer deposited on Si (001) substrate and (b) Ge NHE on NP structure [13]. (b) shows the ideal situation of NHE approach, that means part of the strain energy causes a lateral dilatation of the Si lattice in the pillar; Ge grows pseudomorphically free of defects.

and Ge..

Another approach of strain compensation between Si and Ge is elastic deformation. In the case of planar Ge growth on Si, critical thickness of Ge is several nm only because Si substrate is fixed. However, if part of the strain could be allocated in the Si, the critical thickness will be extended. By fabricating Si nanopillar (NP) or Si nanoisland (NI), more strain could be allocated in the Si because more elastic deformation is possible. By this compliant heteroepitaxy approach, it might be possible to realize an infinite critical thickness for Ge on Si NPs. This theory is proposed in ref. [13]. Here, we review our experimental results of compliance for high quality Ge growth by nanoheteroepitaxy (NHE), which means misfit dislocation-free Ge growth on Si NP or Si NI structures by allocating interface strain also into the Si nanostructures (Fig. 1b).

2. Experimental

Ge NHE is carried out using a single wafer reduced pressure (RP) chemical vapor deposition (CVD) system. The Ge is selectively deposited on Si NPs or Si NIs. The Si NPs and the Si NIs with ~40 nm to ~100 nm diameter are fabricated on standard Si (001) or Si on insulator (SOI) wafers, respectively. To fabricate the Si NPs, double exposure lithography techniques and reactive ion etching (RIE) using Si_3N_4 hardmask is performed [14]. For samples using standard Si substrate, SiO_2 is used for the selective epitaxy as mask on the sidewalls of Si NPs and the Si surface between the Si NPs. To discuss the influence of SiO_2 on the NPs sidewalls, thermally oxidized SiO_2 is used for the first group and SiO_2 deposited by CVD is used for the second group. For samples with thermal SiO_2 sidewall, wet oxidation is performed for the sidewall formation using a Si_3N_4 protection layer on top of Si NPs. For the sample fabrication of Si NPs with CVD SiO_2 sidewalls, CVD SiO_2 deposition is performed after Si NP fabrication to cover the Si NPs and polished by chemical mechanical polishing to open the top of Si NPs. In the case of Si NI fabrication on SOI wafers, the Si NIs are structured by removing Si around Si NIs by RIE etching using a Si_3N_4 hardmask to isolate the Si NIs.

After standard Radio Corporation of America (RCA) cleaning followed by diluted HF treatment, wafers are baked at 850 °C to remove residual oxide on top of Si NPs. After that wafers are cooled down to 300 °C. During the cooling, the carrier gas is changed from H_2 to N_2 at 600 °C to form a hydrogen-free Si surface. After temperature stabilization, Ge is deposited using a N_2-GeH_4 gas mixture for a Ge seed layer. Then the main part of the Ge layer is deposited at 550 °C using a H_2-GeH_4 gas mixture. This two-step Ge epitaxy process is described elsewhere [8,9]. To discuss the compliance effect for different Ge concentrations at the interface, $Si_{1-x}Ge_x$ buffer layer are deposited at 600 °C using H_2-SiH_4-GeH_4-HCl for some samples instead of the Ge buffer layer deposited at 300 °C.

Scanning electron microscope (SEM) is used to analyze the shape of Ge deposited Si nanostructures. Transmission electron microscope (TEM) is used to characterize facets and misfit dislocations in Ge. X-ray diffraction (XRD) and reciprocal space mapping (RSM) are used to estimate the strain distribution in Ge and Si pillars. Synchrotron-radiation energy-dispersive grazing incidence x-ray diffraction is used for the investigation of strain and Ge compositions.

3. Results and discussion

3.1. Selective Ge NHE on Si NP with thermal SiO_2 sidewalls

SEM micrographs of selectively grown Ge on Si NP are shown in Fig. 2 [15]. A cross section TEM image of a NP is inserted. The sidewalls around the Si NP and the Si surface between the NPs are covered by ~10 nm thermal SiO_2. The Ge is grown selectively on top of the Si NP. No Ge nuclei are observed on the sidewalls of SiO_2 and between the Si NPs indicating high selectivity of the Ge growth. On the deposited Ge, pronounced facets of Ge are visible. An irregular shape of Ge NPs with different size of {113} and {111} facets are observed. This is caused by non-uniform strain distribution due to dislocation formation [15]..

RSM of the in-plane (004) Bragg reflection and H scan at K=0 after Ge NHE on Si NP of 40 nm diameter are shown in Fig. 3. The Si (004) peak position at H=4.00 and H=3.84 corresponds to bulk Si and to Ge deposited on Si NPs, respectively. Full relaxation of NHE Ge is confirmed by the H position of the Ge peak. Broadening of the Ge (004) peak in K direction is indicating the presence of twisted

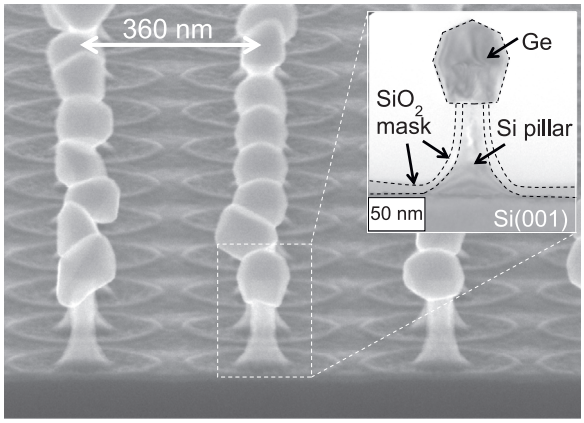

Fig. 2. Angle view SEM image of Si NP after Ge NHE and cross section TEM image (inset). Thermal SiO_2 is used on the sidewalls of the Si NPs [15].