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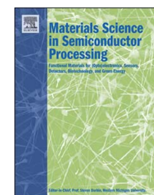

Effect of post annealing on hole mobility of pseudo-single-crystalline germanium films on glass substrates

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ABSTRACT

We examine electrical properties of pseudo-single-crystalline (PSC) Ge films, formed by modulated Au-induced-crystallization (GIC) method, on glass substrates. Although higher growth temperatures and thicker Au layers in GIC conditions degrade the Hall mobility of holes, the influence of the Au deep centers can be ignored. For the thin film transistors, we find that post annealing in N_2 atmosphere enables us to enhance field-effect mobility and the on-off ratios. We discuss the mechanism of the improvement of electrical properties of the PSC-Ge films on the glass substrate.

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1. Introduction

For developing system in displays (SID) [1–3], it is essential to fabricate complementary metal-oxide-semiconductor (CMOS) devices consisting of high-performance thin film transistors (TFTs) formed only by low-temperature processes. Since bulk Ge has relatively high hole mobility compared to bulk Si [4,5], oxide semiconductors [6,7] or organic semiconductors [8–10], we focus on Ge as a channel material in high-performance *p*-channel TFTs [11,12]. Until now, we have succeeded in the synthesis of pseudo-single-crystalline Ge (PSC-Ge) films with extremely large (~600 μm), (111)-orientated, and high-crystallinity grains on glass and plastic substrates by using the modulated Au-induced crystallization (GIC) method [11]. Recently, we also demonstrated the operation of the all-low-temperature (≤300 °C) formed *p*-TFTs with PSC-Ge layers on glass substrates by developing the SiO_2/GeO_2 gate-stack fabrication process [12]. However, the field-effect mobility (μ_{FE}) was largely fluctuated from ~8.2–71 cm^2/Vs, depending on the thickness of the PSC-Ge layers. Also, considering their low on-off ratios ($I_{ON}/I_{OFF} < \sim 33$), we have inferred that the μ_{FE} value is influenced by the interfacial defects between the PSC-Ge layer and the glass (SiO_2) substrate [12].

It is known that the post annealing during solid phase crystallization (SPC) of Ge can affect electrical properties of TFTs on SiO_2 [13]. Kabuyanagi *et al.* demonstrated the remarkable reduction in both the off-current (I_{OFF}) and the threshold voltage (V_{th}) [13], and they inferred the effect of the passivation on the inter-grain defects by the residual oxygen in N_2 or Ar atmosphere. Suh *et al.* [14] reported that additional oxidation at 900 °C after Ge condensation can effectively improve electrical properties of Ge TFTs due to the passivation of the Ge dangling bonds at Ge/SiO_2 interface by oxygen. Also, Yang *et al.* [15,16] have developed a method of Al or Al_2O_3 deposition and subsequent post-deposition annealing, i.e., Al-PDA. With this method, Al atoms diffused into a SiGe layer effectively passivate the electrically active defects, leading to the suppression of I_{OFF} and V_{th}. From these previous works, we should investigate the effect of the post annealing on electrical properties of our PSC-Ge *p*-TFTs. In addition, since our PSC-Ge films are fabricated by using the modulated GIC method, we should also discuss the influence of Au contamination.

In this paper, we study electrical properties of PSC-Ge films on glass substrates by using Hall-bar devices and TFTs. We find that higher growth temperatures and thicker Au layers in GIC conditions degrade the Hall mobility (μ_{Hall}) of holes whereas the influence of the Au deep centers can be ignored. For the PSC-Ge TFTs, post annealing in N_2 atmosphere enables us to enhance field-effect mobility (μ_{FE}) and the on-off ratios. We discuss the mechanism of the improvement of electrical properties of the PSC-Ge films on the glass substrate.

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2. Device fabrication and measurements

The modulated GIC method [11] and fabrication processes of Hall-bars are schematically shown in Fig. 1(a). First of all, an Au layer with a thickness of 50nm was deposited on the glass substrate by an electron-beam (EB) evaporation method at room temperature. Next, a 0.6-nm-thick Al_2O_3 insertion layer was prepared on the Au layer by an atomic layer deposition method at 200°C. After that, the $(a\text{-}Ge/Au)_{20}$ multilayers were formed by an EB evaporation method at room temperature, where the thickness of each a-Ge layer was 2.5nm and the thickness of each Au layer (d_{Au}) was controlled as 0.2, 0.4 and 1.0nm [11]. In order to induce the layer-exchange growth, the samples were annealed at crystallization temperatures (T_c) of 250, 275 and 300°C. All samples were annealed in N_2 atmosphere for 100h, leading to the PSC-Ge films with a d_{Ge} of ~50nm on the glass substrates. The top Au and Al_2O_3 insertion layers were selectively removed by wet etching with a solution containing KI and I_2 [17]. The PSC-Ge films were formed into Hall bars with a length of 20μm and a width of 10μm by using conventional photolithography and dry etching techniques. Here, the Hall bars were located within one PSC-Ge grain. Finally, Au/Ti electrodes were formed by an EB evaporation method.

We also fabricated the accumulation-type *p*-TFTs utilizing the PSC-Ge films formed in an optimized growth condition. The process flow is also schematically illustrated in Fig. 1(b). The detail fabrication process has been described elsewhere; we have already developed a low-temperature (300 °C) fabrication process for the gate-stack structure on Ge(111) [12]. Here, all the TFTs used in this study were fabricated from one PSC-Ge/glass chip with a d_{Ge} of ~50 nm, and the PSC-Ge layer was thinned to a d_{Ge} of < 10 nm by using a chemical and mechanical polishing (CMP) method. In order to investigate the influence of post annealing (PA), we measured electrical properties at room temperature for lots of PSC-Ge TFTs before and after PA. The PA was carried out at 400 °C in N_2 atmosphere for 30 min

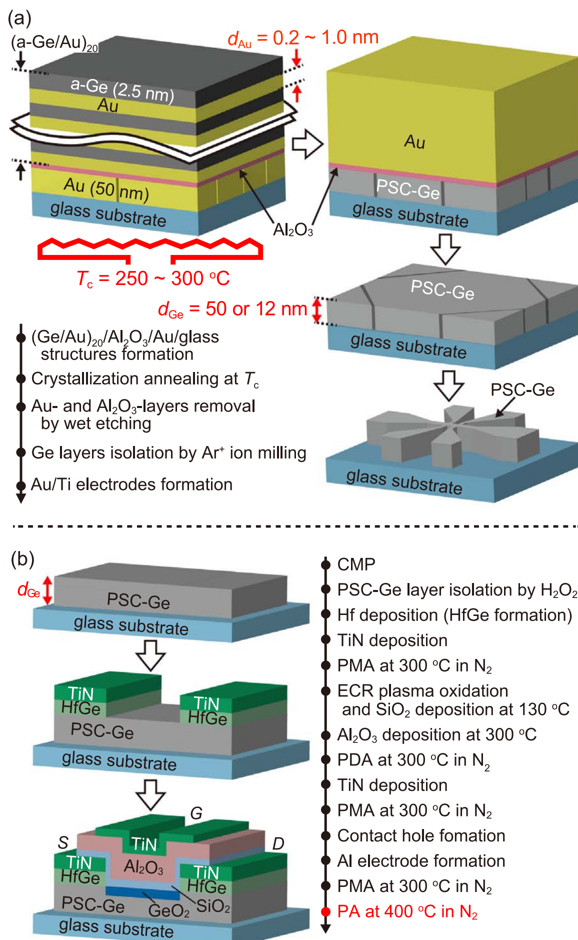

Fig. 1. Schematic illustrations of fabrication processes for (a) Hall bars and (b) TFTs.

Table 1
n_p and μ_{Hall} of the PSC-Ge layers grown at various conditions.

T_c (°C)	300	275	250	250	250
d_{Au} (nm)	0.4	0.4	0.4	1.0	0.2
n_p ($\times 10^{18}$ cm^{-3})	2.4	1.4	1.4	1.8	1.2
μ_{Hall} (cm^2/Vs)	101	146	170	120	210

3. Results and discussion

3.1. Influence of growth conditions on Hall mobility

The hole carrier density (n_p) and μ_{Hall} of the PSC-Ge layers were estimated from the Hall-effect and longitudinal resistance measurements at 300 K. The results are summarized in Table 1. For the PSC-Ge layers formed by using $d_{Au} = 0.4$ nm, we can find that low-temperature growth ($T_c = 250$ °C) is effective to obtain low n_p and high μ_{Hall}. When we change d_{Au} from 0.2 to 1.0 nm at $T_c = 250$ °C in an $(a\text{-}Ge/Au)_{20}$ multilayer, it seems that electrical properties can be improved with decreasing d_{Au}.

Here we present optical micrographs of the PSC-Ge layers with $d_{Au} = 0.4$ grown at $T_c = 250$ and 300°C in Figs. 2(a) and (b), respectively. The size of Ge grains of the PSC-Ge layer grown at $T_c = 250$°C is relatively large compared to that grown at $T_c = 300$°C. Thus, we should use lower T_c and smaller d_{Au} to obtain available Ge grains for TFTs on the glass substrate.

For the PSC-Ge layer grown in the optimum condition, i.e., $d_{Au} = 0.2$ nm and $T_c = 250$ °C, we also investigated the dependence of n_p on temperature (T) and plotted $\log(n_p)$ versus $1000/T$, as shown in Fig. 3 (blue open circles). We can see that the n_p weakly decreases with increasing $1000/T$ (decreasing T). This tendency is the same as that on a flexible substrate shown in a previous work [18]. Here we discuss the contamination of Au in the PSC-Ge films because the PSC-Ge films were formed by the GIC method. We should reconsider the inclusion of Au as an accepter impurity for Ge. The values of the acceptor levels (E_A) for Au in Ge have been reported as 0.15, 0.47 and 0.60 eV [19]. The relationship between n_p and E_A can be approximately given [20] by

$$n_p \propto \exp\left[-(E_A - E_V)/2k_BT\right], \tag{1}$$

where E_V is the energy level of valence band edge and k_B is the Boltzmann's constant. In Fig. 3, we also show n_p–$1000/T$ curves with $E_A = 0.15$ (black), 0.47 (green) and 0.63 eV (purple), calculated from Eq. (1). We find that our data is not consistent with the features of the well-known Au acceptors [19]. Using Eq. (1), we can also estimate E_A from our raw data. The linear fitting curves shown mean that the E_A value of the PSC-Ge film ($d_{Ge} = \sim 50$ nm) is estimated to be ~0.03 eV. This value is very shallow and is not associated with deep accepter levels due to the Au contamination in Ge.

Also, we fabricated the Hall-bar device with $d_{Ge} = \sim 12$ nm, where the PSC-Ge layer was thinned from ~50 nm to ~12 nm by using a CMP method. The Arrhenius plot of n_p for the device with $d_{Ge} = \sim 12$ nm is also shown in Fig. 3 (red open square). The estimated E_A value is also ~0.03 eV. From these considerations, we have ruled out the influence of Au impurities forming deep-

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