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Tensile strain ultra thin body SiGe on insulator through hetero-layer transfer technique

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ABSTRACT

The ultra thin body (UTB) SiGe on insulator (SGOI) substrate with body thickness of only 5 nm has been fabricated by hetero-layer transfer technique with highly selective wet etching. According to Raman spectroscopy, UTB-SiGe layer with Ge fraction of 67% and +1% partially tensile strain was transferred onto the SiO_2/Si host substrate without the strain degradation. To present the feasibility of UTB-SGOI substrate, a well-behaved performance of 2-μm-gate-length normally off UTB-SGOI nMOSFET has also been demonstrated.

1. Introduction

As the demand increases for higher performance and lower power consumption devices, new channel materials and novel device structures are inevitable to be implemented to the current CMOS technology. Strained $Si_{1-x}Ge_x$ alloy with high Ge fractions is promising for replacing present Si channel owing to the enhanced carrier mobility for both electrons and holes [1]. As compared with the pure Ge channel, Ge rich $Si_{1-x}Ge_x$ alloy is more prone to suppress the band-to-band tunneling owing to the wider band gap [2]. For better gate control and suppressed short channel effects in the ultimately scaled devices, the fully depleted ultra thin body (UTB) Si-on-insulator (SOI) structure is a potential option. Therefore, it is of interest to combine the advantages of the strained SiGe channel and the UTB-SOI structure to realize a UTB SiGe-on-insulator (SGOI) substrate as a high functional platform for fabricating device. Recently, IBM and CEA-Leti have both imported UTB-SGOI substrates as starting materials for the ultimate CMOS devices [3,4].

To realize SGOI substrate, several approaches such as Smart-Cut™ technology [5,6], liquid phase epitaxy [7,8], and Ge condensation technique [9–11] have been proposed. However, most SGOI layers fabricated so far are usually too thick and/or with high defect density. Recently, we have developed a low temperature (< 400 °C) layer-transfer technique called Epitaxial-Lift-Off (ELO) [12,13] for fabricating high quality UTB-GeOI substrates. This technique can be applied to transfer a desired epitaxial layer onto the host substrate. For example, strained SiGe/Ge heterostructures can be transferred onto SiO_2/Si substrate while preserving the strain throughout the layer-transfer process. Although there have been many reports on fabricating highly compressive strained SGOI substrates [10,14,15], UTB-SGOI substrates with tensile strain, resulting in possible enhanced electron mobility, have been rarely reported.

In this work, tensile strained UTB-SGOI substrates have been fabricated by using hetero-layer transfer technique. Taking advantages of SiGe/Ge heteroepitaxial growth and highly selective wet etching, the SiGe layer can be transferred onto the SiO_2/Si substrate with precise thickness control. Raman spectroscopy, atomic force microscopy (AFM), scanning transmission electron microscopy (STEM), and Hall effect measurement were employed to characterize the fabricated UTB-SGOI substrates. To present the feasibility of UTB-SGOI substrates, UTB-SGOI nMOSFETs were also fabricated. Because of the attainment of uniform and conformal UTB-SiGe layers, the UTB-SGOI nMOSFETs can be realized by using ion implantation after germanidation (IAG) technique [16], which is a low thermal budget process; thus helps to maintain the strain of UTB-SiGe layers.

2. Experimental procedures

Fig. 1 is a schematic flow for fabricating tensile strain UTB-SGOI substrate by hetero-layer transfer technology. The epitaxial strained SiGe/Ge/AlAs/GaAs heterostructures were grown by low-pressure CVD. The Ge fractions and thickness of SiGe layers were designed by considering the compromise between critical thickness and strain relaxation. After ALD Al_2O_3 deposition, the wafers were patterned into

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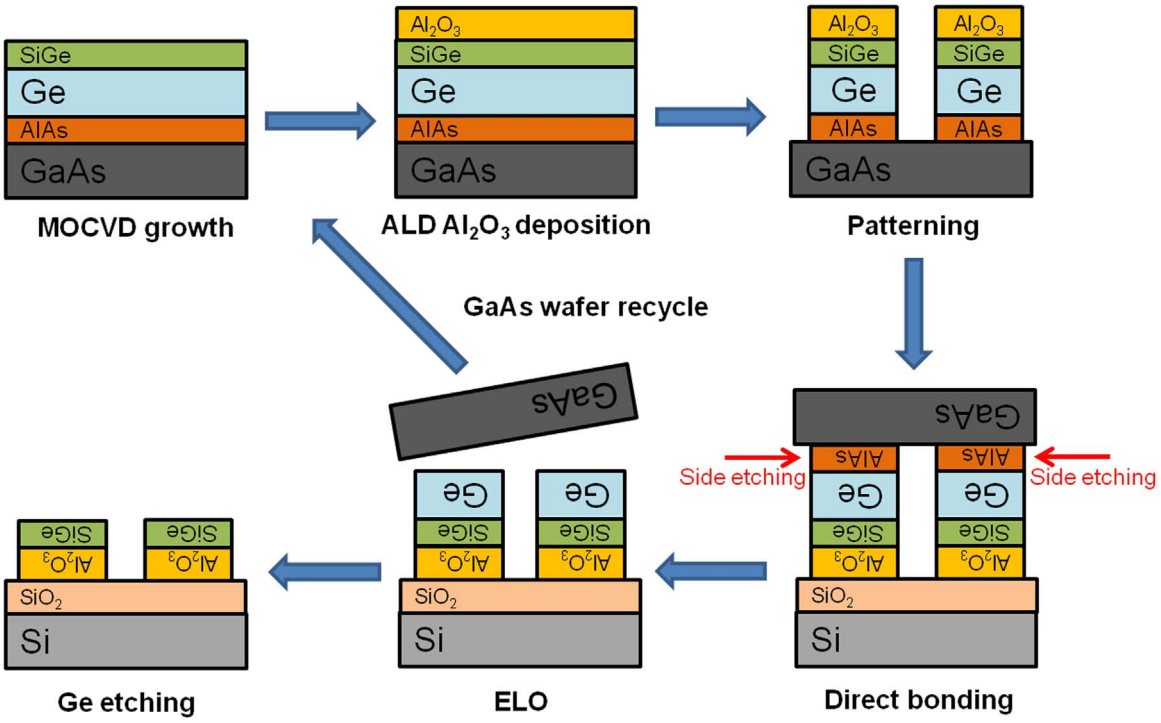

Fig. 1. Schematic flow of hetero-layer transfer process for fabricating tensile strain UTB-SGOI substrate.

stripe shapes using lithography, and then the epitaxial layers were dry etched by reactive ion etching (RIE) down to AlAs layer, which acted as a splitting layer later. Subsequently, the direct bonding with SiO_2/Si host substrate was performed in the press machine under vacuum. To release GaAs substrate, the AlAs layer was selectively and laterally etched by HCl solution at room temperature. The released GaAs substrate can be recycled as a donor wafer in the first step for hetero-epitaxial growth. Finally, the top Ge layer was etched selectively in HCl/H_2O_2 mixed solution, which is an important step of this hetero-layer transfer technology. To characterize the quality of the transferred SiGe layer, we used 488 nm lasers Raman spectroscopy, AFM, and STEM. The Hall mobility of the transferred SiGe layer was also extracted by Hall effect measurement with four points probe resistance measurement at room temperature.

We also fabricated strained SiGe channel MOSFETs using UTB-SGOI substrate. After SiGe active areas isolating by RIE, the samples were covered with 5 nm Al_2O_3 by ALD using trimethylaluminum (TMA) and O_2 plasma as precursors. Subsequently, TaN was deposited by sputtering and formed into gate electrodes by RIE. Then, the self-aligned metallic NiGe S/D regions were formed by low thermal budget ion implantation after germanidation (IAG) process. The detail of IAG process was described elsewhere [16]. Finally, the Ti/W/Al metal stacks were deposited by sputtering and an e-beam evaporator, respectively, as measurement pads.

3. Results and discussion

To precisely determine the etching rate of Ge as well as the strained SiGe in HCl/H_2O_2 mixed solution, Ge (~400 nm)/SiGe (6.5 nm)/Ge (~100 nm) sandwiched structure was used where the strain of SiGe maintain during the etching process due to the existence of underlying Ge layer. The etching depth profile as a function of etching time is shown in Fig. 2. A linear trend of the etching depth during Ge layer etching was obtained while a very slow etching behavior was observed during strained SiGe layer etching. The slope of the blue and the red dash line represents for the etching rate of Ge and strained SiGe in the mixed solution, respectively. As a results, high etching selectivity of around 30 between Ge and strained SiGe in HCl/H_2O_2 mixed solution enables us to remove the top Ge layer without thinning SiGe underneath.

Raman spectroscopy has been extensively used to verify the crystallinity of SiGe throughout the layer-transfer process as well as the strain in SiGe layer. Fig. 3 shows the Raman spectra of (a) the as-grown SiGe/Ge/AlAs/GaAs heterostructure, (b) the epitaxial SiGe layers after RIE and (c) the layer-transferred SiGe. The corresponding structures for Raman analysis are also shown in the inset of Fig. 3. The domain peak at 288 cm^{-1} and 399 cm^{-1} corresponds to the Ge-Ge and Si–Ge phonon band from the SiGe layer, respectively. Aside from the main peaks, the additional phonon peak observed at 300 cm^{-1} in Fig. 3(a) and (b) is associated with Ge-Ge modes of the underlying relaxed Ge layer. After patterning the donor wafer, there were no significant changes in Raman spectrum. However, it is observed that the relaxed Ge-Ge peak vanished and only the strained Ge-Ge and Si–Ge mode

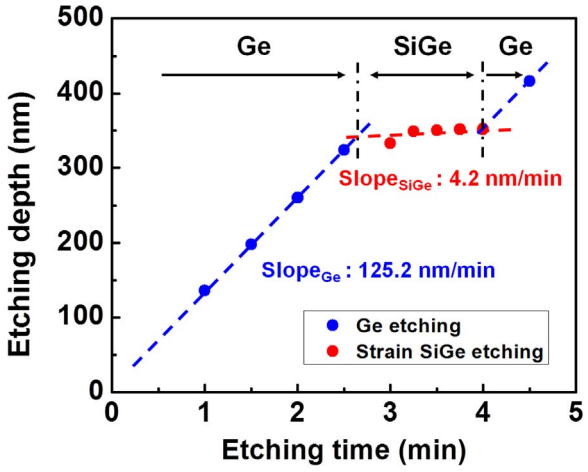

Fig. 2. The etching depth profile of Ge (~400 nm)/SiGe (~6.5 nm)/Ge (~100 nm) sandwiched structure in HCl/H_2O_2 mixed solution. The slope of the blue and the red dash line represents for the etching rate of Ge and strained SiGe in the mixed solution, respectively.