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Performance analysis of nanoscale GeSn MOSFETs for mixed-mode circuit applications

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ABSTRACT

Using extensive numerical analysis we investigate the impact of Sn ranging 0–6% in compressively strained GeSn on insulator (GeSnOI) MOSFETs for mixed-mode circuit performance at channel lengths (L_g) ranging 100–20 nm with channel thickness values of 10 and 5 nm. Our results reveal that 10 nm thick $Ge_{0.94}Sn_{0.06}$ channel MOSFETs produce improvement of peak transconductance g_m, peak gain Av, peak cut-off frequency f_T and maximum frequency of oscillations f_{max} by 80.5%, 18.8%, 83.5% and 81.7%, respectively compared with equivalent GeOI device at L_g = 20 nm. Furthermore, such devices exhibit 78.8% increase in ON-current I_{ON} while yield 44.5% reduction in delay as compared to Ge control devices enabling them attractive for logic applications. Thinning of the channel thickness from 10 to 5 nm increases peak *Av*, peak transconductance efficiency and reduces output conductance and OFF-current I_{OFF} while degrading other parameters in all GeSnOI and control Ge devices.

1. Introduction

Recently, the germanium–tin (GeSn) alloys have emerged as promising materials for optoelectronics and also for high performance nanoscale CMOS transistors owing to their tunable bandgap [1] and outstanding electron and hole mobilities [2]. Furthermore these alloys are rapidly expanding their applications in constructing tunnel field effect transistors [3–7] which are promising for low power logic circuit design. The incorporation of Sn in Ge reduces the energy separation between the indirect (L) and direct (Γ) conduction band valleys enabling the alloy nearer to a direct bandgap material. Earlier findings predicted that the transition between indirect to direct occurs at 6 − 8% of Sn [8,9]. Since the lattice constant of Sn is 15% larger than that of Ge, an epitaxial GeSn layer grown on Ge is subjected to a biaxial compressive strain, which enhances the hole mobility in the GeSn layer [8,10–15]. This remarkable property has sparked researcher to fabricate high performance pMOSFETs using a GeSn channel.

Although there have been extensive studies on Ge based CMOSFETs with a view to replacing the long standing Si [16–19], investigations on GeSn film growth, CMOS device fabrication using them and GeSn based circuit performance are still in their infancy. Literature screening shows some reports demonstrating the growth techniques of $Ge_{1-x}Sn_x$ such as low temperature molecular beam epitaxy [20], chemical vapor deposition [21], and solid phase epitaxy [22]. More recently high quality, low-defect density GeSn films are epitaxially grown on top of strain-relaxed Ge virtual substrate which have become the preferred platform for MOSFETs using GeSn channel. Notably Gupta et al. reported that $Ge_{0.97}Sn_{0.03}$ exhibits enhancement in effective hole mobility as compared to control Ge by 85% in high inversion charge regime [10]. Some researchers [14,23] demonstrated 66% higher hole mobility in $Ge_{0.947}Sn_{0.053}$ pMOSFET compared with that in Ge pMOSFET. Recent studies reported the record high hole mobility of 845 $cm^2V^{-1}s^{-1}$ for undoped $Ge_{0.92}Sn_{0.08}$ quantum well pMOSFETs [15,24,25]. Also, there has been a report in [26] on the injection velocity of carriers in Ge and GeSn channels with 6% and 10% of Sn. Very recently fabrication of pTFETs using high quality ultra-thin GeSn film on Si was reported, which exhibited excellent hole mobility, steep subthreshold swing and ON-current to OFF-current ratio as high as 10^7 [5]. Moreover, there is an experimental demonstration on high hole mobility obtained by optimizing capacitor thickness of a CVD-grown GeSn QW MOSFET with a low thermal budget ~400 °C [27]. However, less attention has yet been paid to study the impact of Sn contents in GeSn channel, and the channel thickness on the device parameters for such devices associated with mixed-mode signal applications.

In this paper, we have performed detailed investigations on the various device parameters related to analog and logic circuit applications for strained GeSnOI MOSFETs having various mole fractions of Sn, channel lengths and channel thicknesses. In the present study, device parameters in analog domain include transconductance, output conductance, voltage gain, unity gain cut-off frequency and maximum

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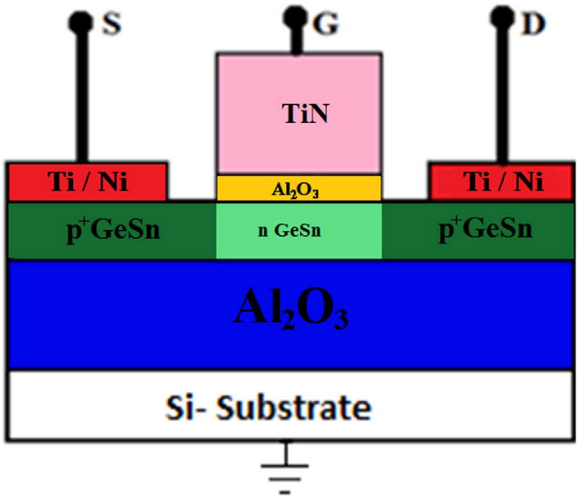

Fig. 1. Illustration of GeSnOI p-channel MOSFET with Al_2O_3 as the gate dielectric. Ti/Ni is used to form source/drain contacts and TiN serves as the gate metal.

frequency of oscillations while parameters related to logic performance are ON-current, OFF-current and intrinsic switching delay. Moreover, different device parameters of GeSnOI devices associated with analog and logic applications are compared with the corresponding parameter of the control GeOI device. Our findings reveal that GeSn devices outperform Ge devices with reference to all the above- noted device parameters related to analog and logic applications.

2. Device structure and simulation parameters

In the present study, we consider the GeSn-on-Insulator MOSFET structure as shown in Fig. 1. GeSnOI on Si wafers may be formed using direct wafer bonding (DWB) technique following the approach similar to that described in [28]. This process involves atomic layer deposition (ALD) of Al_2O_3 on top of the handle wafer. For the donor wafer, GeSn may be grown pseudomorphically on a Ge buffer placed on $GeO_2/SiO_2/Si$. Subsequent to that atomic layer deposition of a 2 nm thick Al_2O_3 is conducted on top of the GeSn layer. Then DWB is carried out between two ALD Al_2O_3 layers exploiting their hydrophilic properties followed by selective etching. The gate metal TiN may be sputter deposited with subsequent patterning followed by low temperature annealing using forming gas. Finally, source/drain contacts may be formed using Ti/Ni metal deposition. Notably, earlier findings [28] pointed out that the reduction of compressive strain occurs due to high temperature of post bonding annealing and wide difference in thermal expansion coefficients of SiO_2, Ge and Sn [28]. It may be noted that the thermal expansion coefficients of Ge, Sn, SiO_2 and Al_2O_3 are reported to be $6\times10^{-6}\,K^{-1}$, $2.34\times10^{-5}\,K^{-1}$, $5.6\times10^{-7}\,K^{-1}$ and $5–6\times10^{-6}\,K^{-1}$, respectively [29–31]. In our proposed scheme since the temperature of post bonding annealing is low and the difference between thermal expansion coefficients of Al_2O_3 [31] and Ge is marginal, with small amounts of Sn it is more likely that the pseudomorphic compressive strain in the GeSn wafer will be retained. We consider devices featuring channel length L_g variation ranging 100–20 nm along with the channel thickness of 5 and 10 nm. Table 1 lists various device design parameters of GeSn MOSFETs and supply voltage, which are chosen in accordance with the specifications in the International Technology Roadmap for Semiconductors [32].

We employ the numerical device simulator, SILVACOATLAS [33] to simulate fully depleted GeOI and GeSnOI pMOSFETs. The interface trapped charge density D_{it} values at the front and back surfaces are chosen following the experimental findings on Al_2O_3/GeSn interface reported in [9]. Incorporation of Sn in the GeSn channel introduces compressive strain which may be conveniently expressed in terms of Sn

Table 1
Various parameters of GeSn MOSFET shown in Fig. 1.

Symbol	Parameter	Value
W	Channel width	1 μm
t_{ox}	Gate oxide (Al_2O_3) thickness	2 nm
t_{box}	Box oxide thickness	460 nm
N_D	Substrate doping concentration	$6.8\times10^{16}\,cm^{-3}$
N_A	p-type source/drain doping concentration	$10^{19}\,cm^{-3}$
Q_f	Fixed oxide charge density	$10^{-7}\,C\,cm^{-2}$
D_{itf}	Front gate interface trapped- charge density [9]	$2\times10^{12}\,eV^{-1}\,cm^{-2}$
D_{itb}	Back gate interface trapped- charge density [9]	$2\times10^{12}\,eV^{-1}\,cm^{-2}$
V_{DD}	Supply voltage	−0.8 V
$q\phi_m$	Metal work function	4.6 eV

contents or it may be calculated using the expression $\varepsilon = -\ 0.166x/(1+0.166x)$, where x is the mole fraction of Sn in GeSn [34]. In this work we represent strain with molar contents of Sn in the GeSn layer as is presented in numerous articles in literature. The strain impacts band gap and band structure of GeSn, which in turn influences effective mass of electrons and holes, and also their mobility. We take into account the effects of strain in GeSn channel due to incorporation of 0–6% of Sn while computing the various material parameters such as bandgap, dielectric constant and electron affinity and transport parameters like effective mass of electrons and holes, density of states DOS, carrier concentration and mobility. The bandgap widening of the GeSn channel with reduced channel thickness due to carrier localization effect is considered. Experimental findings reveal [35,36] that the energy gap, E_g in $Ge_{1-x}Sn_x$ semiconductor alloys exhibits a non-linear dependency on alloy composition x. The band gap of $Ge_{1-x}Sn_x$ semiconductor alloy is typically calculated using the following expression

$$E_g^{Ge_{1-x}Sn_x} = (1-x)\,E_g^{Ge} + xE_g^{Ge} + x(1-x)b_g\,, \tag{1}$$

where b_g is called the band gap bowing parameter and the resulting 'bowing' parameters for direct and indirect band gaps are found as 2.3 eV and 4 eV, respectively, for the best fit with the Sn composition ranging 0–6%. The bandgap of the ultrathin GeSn channel is computed using the band structure simulator available in nanohub [37] and verified by the reported experimental data for Ge [38]. The lattice constant of GeSn alloy is estimated as

$$a^{Ge_{1-x}Sn_x} = (1-x)\,a^{Ge} + xa^{Ge} + x(1-x)\alpha_c\,, \tag{2}$$

where α_c is the lattice bowing parameter and is found to be equal to −0.166 Å. The dielectric constant and electron affinity of $Ge_{1-x}Sn_x$ are computed using weighted linear interpolation between corresponding quantities of Ge and Sn.

The intrinsic carrier concentrations in the channel are calculated taking into account the effect of strain and carrier localization effect due to ultra thin channel. The different components of effective mass of electrons and holes are extracted directly from the conduction and valence band edges, respectively, using a parabolic fit. The electron density of states (DOS) effective masses at Γ-valley and L-valley are calculated as

$$m^*_{e,\,DOS}(\Gamma) = m^*_e(\Gamma) \text{and} m^*_{e,\,DOS}(L) = [g^2(m^*_{e,\,t})^2 m^*_{e,\,l}]^{1/3}, \tag{3}$$

where $m^*_{e,DOS}$ (Γ) and $m^*_{e,DOS}$ (L) are the DOS effective masses of electrons in Γ and L valleys, respectively. m^*_e (Γ) is the isotropic effective mass of electrons in Γ-valley and $m^*_{e,t}$ and $m^*_{e,l}$ are the transverse and longitudinal effective masses of electrons in the L-valley, respectively. GeSn alloy exhibits 8 fold degenerated < 111 > L valleys for electrons. The hole DOS effective mass $m^*_{h,DOS}$ *(L)* is computed using the following expression

$$m^*_{h,\,DOS}(L) = [(m^*_{hh})^{3/2} + (m^*_{lh})^{3/2}]^{2/3}, \tag{4}$$

where m^*_{hh} and m^*_{lh} are the heavy hole and light hole effective masses, respectively. m_0 is the free electron effective mass.