



Influence of pre-polishing process on site flatness values of polished wafers



Genghang Zhong^{a,b,*}, Yongduo Ning^b, Qigang Zhou^a, Yongzhi Bian^b, Xin Wang^b, Xiang Qu^b,
Lei Wang^b, Erjing Zhao^b

^a General Research Institute for Nonferrous Metals, Beijing 100088, China

^b GRINM Semiconductor Materials Co., Ltd., Beijing 100088, China

ARTICLE INFO

Keywords:

SFQR
Etching
Grinding
CMP (chemical mechanical polishing)

ABSTRACT

The preparation of semiconductor silicon polished wafer is a multi-stage manufacturing process. This paper analyzed the influence of polished wafers' SFQR (Site flatness front least square range) values with different pre-polishing process. In this study, the pre-polishing processes included dual-side lapping & etching, dual-side grinding and back-side polishing. Among them, the etching process was divided into caustic etching and acid etching with different removal amount and different rotation speed. The experimental results show that different pre-polishing processes have significant effects on SFQR values of polished wafers. Caustic etching, dual-side grinding and back-side polishing are more suitable for polished wafer's SFQR, while the center area of acid etching wafers show worse polished wafer's SFQR due to the etching mechanism.

1. Introduction

Due to the sharply increasing demand of automotive electronics, consumer electronics and IoT (Internet of Things) markets, 200 mm silicon wafer's market steadily enlarge in demand. Advanced requirements for 200 mm wafer technology was extended into 0.13 μm beyond. SFQR is one of the key parameters which correlates to lithography process of IC (Integrated circuit) fabrication. It is very difficult to realize SFQR value as small as 0.13 μm for 200 mm silicon wafers. Nowadays, 200 mm silicon wafers are commonly using single-side polishing technology. To meet these flatness requirements, there is still a lot of research space.

To obtain high flatness silicon wafers, we need to control the polishing material removal rate and removal non-uniformity [1,2]. According to the Preston equation [3]:

$$MRR = K_e PV \quad (1)$$

MRR (Material removal rate) mainly depends on the polishing pressure of the polishing process and the relative velocity between the wafer and the polishing pad. In addition, the characteristics of consumables in polishing process and the macroscopic and microscopic appearance of the wafer before polishing also have great influence on material removal rate. All the factors are combined to influence the polishing removal rate. There are many interactions in the polishing process, such as the contact of the polishing slurry particles with the surface of the silicon wafer, the bonding state of the polishing pad with the silicon wafer, the contact of the polishing slurry particles with the

polishing pad. The material removal non-uniformity expression is [4]:

$$\begin{aligned} WTWNU &= \frac{K_e(PV)_{\max} + MRR_0 - K_e(PV)_{\min} - MRR_0}{K_e(PV)_{\text{avg}} + MRR_0} \\ &= \frac{K_e[(PV)_{\max} - (PV)_{\min}]}{MRR_{\text{avg}}} \quad (2) \end{aligned}$$

The distribution of pressure, the distribution of relative velocity, the distribution of temperature, the flow of polishing fluid, and the properties of the polishing pad all have a large effect on polishing removal non-uniformity.

Most of the ongoing research on the polishing effect of silicon wafers focuses on the chemical mechanical polishing process itself, which includes the properties of the polishing pad [1,5,6], polishing slurry properties [7], the control of slurry flow [8] and the study of abrasive behavior during polishing [9–11], also, there are studies on polishing removal mechanism and theoretical model [12–14], and kinematics analysis of polishing process [15,16]. The effects of pre-polishing processes include dual-side lapping, etching, dual-side grinding and the wafer's shape before polishing are also discussed [17–22]. In addition, the influence of the process integration on the polishing results is also a research direction. Based on the above studies [23–25], this paper will further study the effects of the pre-polishing processes and the process integration on the SFQR value of polished wafers.

In this paper, a series of experiments are carried out to study the effects of different pre-polishing processes which can significantly affect the SFQR value of polished wafers.

* Corresponding author at: General Research Institute for Nonferrous Metals, Beijing 100088, China.

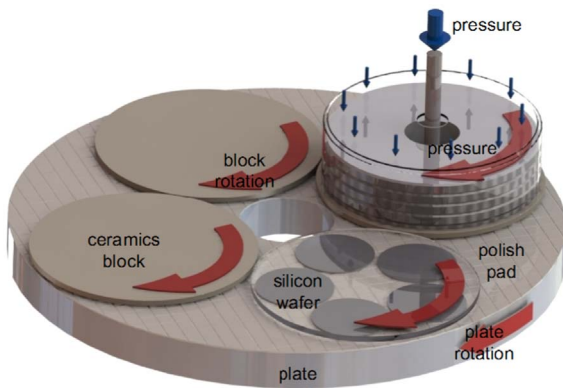


Fig. 1. A sketch of the typical polishing equipment.

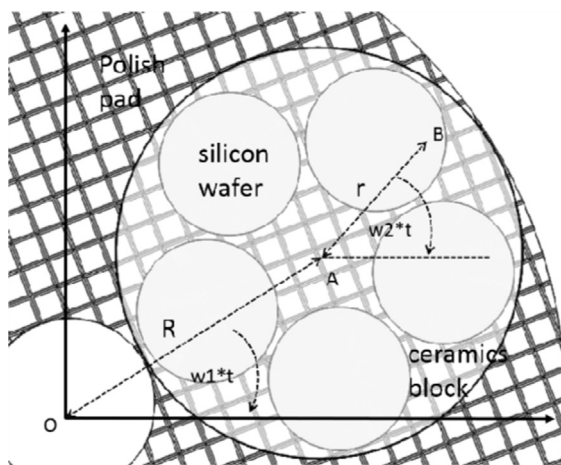


Fig. 2. A sketch of the polishing motion.

1.1. The kinematic analysis of polishing

The chemical mechanical polishing is usually applied to obtain the mirror surface with high flatness and smoothness. The sketch of the typical polishing equipment is shown in the Fig. 1. Fig. 2 shows the necessary parameters to analyze the polishing motion.

The path curve equation of any point on the silicon wafer which is relative to the polishing plate is shown in the Eq. (3) [26].

$$\begin{cases} x = R \cos \omega_1 t + r \cos \omega_2 t \\ y = R \sin \omega_1 t + r \sin \omega_2 t \end{cases} \quad (3)$$

Respectively, take different rotation speed of polishing plate and pressure head, obtain the corresponding motion trajectory by simulation, the results are shown in the Fig. 3.

When the rotation speed of the pressure head is the same with the polishing plate's, any point on the silicon wafer has the same path shape which is regular circle shape and the length of the path curve is same, which ensures the uniformity of velocity distribution on the silicon wafer.

1.2. Mechanical analysis of polishing process

According to the Preston equation, pressure plays an important role in material removal during the polishing process. As we can see from the Fig. 4, there are two mainly layers of film in the polishing system, one is the thin layer of wax between the silicon wafer and the ceramic block, the other layer is the liquid film between the wafer and the polishing pad. There are two pressure sources exerted on the ceramic block, one is from the pressure head and the other is from the counterweight. The pressure from the pressure head is applied to the center

area of the ceramic block and the pressure values are non-uniform distribution from the center area to the edge. To make the polishing pressure applied uniformly to the back side of the wafer, the counterweight is needed. The stress from the counterweight is applied to the periphery area of the ceramic block. Under the interaction of these two pressures, the pressure distribution on the ceramic block achieves a dynamic equilibrium and the pressure distribution on the ceramic block is uniform.

In the theory, by adjusting the process parameters, a balance would be found between pressure and relative velocity, as a result, the front surface of the silicon wafer can be uniformly shaped. After polishing, the front surface of the silicon wafer will be smooth and precisely flat. But in fact, the SFQR parameter after polishing is always poor. This is mainly because polishing is not only affected by the process parameters of the polishing process but also affected by the morphology of wafer's surface. In order to investigate the effect of wafer's surface morphology on the SFQR, a series of experiments involving pre-polishing processes in silicon substrate wafer manufacturing system were carried out.

2. Experiment

2.1. Experimental materials and equipments

The silicon wafers used in the experiment were 200 mm light boron-doped < 100 > wafers. The resistivity of these wafers was 15–20 Ω cm. These silicon wafers were divided into groups according to their thicknesses, and the difference in the thickness of the wafers within each group during polishing was less than 1 μ m. In the polishing process, the rotation speed of polishing plate and pressure head is the same, and the speed is 30r/min. The general flow of the experiment is shown in Fig. 5. The geometric parameters of the silicon wafer are tested at each step in the experimental flow. The tools used in the experiment includes double-side lapping machine, acid etching machine, caustic etching machine, double-side grinding machine, single-side polishing machine and geometric parameters testing equipment. The polishing treatment is carried out in a state in which the polishing pad is in good condition and the polishing machine is sufficiently heated.

2.2. The experimental process

2.2.1. The research of effect on polished wafer's SFQR with different etching types

The silicon wafers were divided into two groups. Respectively, caustic etching or acid etching treatment was carried out to complete remove the damage layer produced by dual-side lapping. The two etching sheets were then polished together under the same process conditions. Every wafer's geometric parameters were tested before and after polishing.

2.2.2. The research of effect on polished wafer's SFQR with different acid etching process variable

Acid etching process has many process conditions variables. Changes in each process conditions are likely to cause different effect on etching results which in turn will affect the polishing output. In this paper, we discussed the effect of different removal amount and different rotation speed on polished wafer's SFQR.

2.2.2.1. The research of effect on polished wafer's SFQR with different etching removal amount. The silicon wafers were divided into three groups. Using the same acid etching process conditions, the silicon wafers were removed 15 μ m, 20 μ m and 30 μ m respectively. The three etching sheets were then polished together under the same process conditions. Every wafer's geometric parameters were tested before and after polishing.

2.2.2.2. The research of effect on polished wafer's SFQR with different

Download English Version:

<https://daneshyari.com/en/article/5006007>

Download Persian Version:

<https://daneshyari.com/article/5006007>

[Daneshyari.com](https://daneshyari.com)