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Single lithography-step self-aligned fabrication process for Vertical-Cavity Surface-Emitting Lasers

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ABSTRACT

We demonstrate a self-aligned process to fabricate Vertical-Cavity Surface-Emitting Lasers (VCSEL) which combines, within a single lithographic step the mesa etch, the surface passivation, the opening of the emission window and the top annular metallization. This process flow, based on a double photoresist layer enabling two lift-off steps, offers great advantages such as easy and fast implementation while insuring a perfect alignment between the emitting window, the passivation layer aperture and the metal-ring contact. VCSEL fabrication is drastically simplified and its repeatability improved. Finally, this process can be advantageously applied to other photonic devices such waveguide-ridge lasers, modulators, LED, etc.

With the global increase of the data communication traffic, there is an ever-increasing demand for VCSELs sources to be used in datacenters to further expand the use of fast optical communications channels between supercomputers and routers [1].

In addition to this mainstream application, VCSEL are also rapidly expanding in diversifying sensing applications including optical mouse, and smart sensors for mobile devices, atomic clocks, surgery, and for imaging and gesture recognition mass-market products.

- Thus, the simplification and the enhancement of the reliability of VCSEL devices manufacturing, is highly coveted by industrial manufacturers to ensure their rapidly expanding mass-production capacities.
- The commonly-used VCSEL process fabrication flow, requiring four lithography steps with precise mask alignments between them, consists in the following main stages:
- First, an annular top contact is defined by a metal lift-off.
- Then, a first lithographic alignment is done to form an etching mask for the mesa definition [2].
- Next, surface passivation is realized by a plasma-assisted dielectric deposition, followed by a new tight mask alignment [3] to define the transparent emission window. This window opening is done by etching the passivation layer with a chemical solution or by dry etch. Besides the risk of lateral misalignment, both selective etching methods can be problematic with a possible under-etch of the passivation layer with the chemical method, or damaging the top VCSEL semiconductor layers because of the lack of selectivity for the dry etch [3,4], resulting in deteriorated VCSEL performances.
- Finally, the last lithography step and alignment is realized for the lift-off of the metallic top contact-pad.

The solution proposed in this paper consists in drastically simplifying this above process flow by performing all of these steps by applying only one lithographic step instead of four, and thus without any required mask alignment. To do so, a suitable T-shaped double-layer photoresist is used for successively achieving the VCSEL mesas etching by Induced Coupled Plasma – Reactive Ion Etching (ICP-RIE), the sidewalls passivation with SiO_x layer by PECVD and emission window opening by a first lift-off, and finally, completing the process by the top metal contact lift-off. This innovative self-aligned process enables a very fast and straightforward process flow. In addition, the metal overlap on the top-mesa emitting window is easily controlled during the process.

This sequence of processing steps is greatly facilitated by low-temperature plasma-assisted deposition of the passivating dielectric layer (SiO_x or Si_xN_y), since a lift-off technique can be utilized for releasing the emission opening window on top of the mesa.

Several new plasma-based deposition techniques (ICP-PECVD,

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ECR-PECVD) have been developed over the past decades, in order to realize high quality SiN_x [5], SiO_x [6], or a-SiH layers with a good control of their stress and their optical and electronic properties.

These capabilities of depositing passivating SiN_x or SiO_x films, around 100 °C and even at room temperature offer many opportunities to use structured polymer coating on the wafer surfaces and thus to apply a lift-off technique for surface patterned coating [7]. In addition, thanks to a wide range of possible parameters to control the plasma, more or less conformal coatings on the profiled surfaces can be achieved.

The lift-off techniques have then been advantageously used in diverse applications, such as MEMS, III/V microelectronics and optoelectronics components, optical sensors, etc. However, most of the works in the literature on dielectric lift off was reported on SiN_x, and only to a minor extent on SiO_x.

In 2001, Suchanek et al. demonstrated a lift-off of a Si_xN_y:H optical coating after standard PECVD deposition at 80 °C, showing good optical properties and long-time stability [8]. More recently, in 2007 for MEMS applications, Vanhove et al. studied the properties of Si_xN_y layers with low H-content deposited by ICP-PECVD at 100 °C and lifted-off thanks to a double-layer composed of LOR3A – non photosensitive – and ECI photoresist [9].

In the case of SiO_x coatings, early works [10,11] reported a lift-off patterning method, requiring an intermediate chemical etching step of the SiO_x deposited on the edge sidewalls of the resist patterns.

Later on, undercut resist profiles were successfully applied to lift off Si_xN_y ECR-PECVD deposited layers, in a very similar way to standard metal lift-off techniques [7]; enabling the lift off of more than 1 μm thick Bragg mirror stacks [12].

Then, some authors proposed to combine, with one single resist patterned coating, the lift off of dielectric coating and other technological steps, such as ion implantation, etching or/and metallization steps [13–15].

This combination of dielectric lift-off and other processing steps then enables self-aligned fabrication process, particularly of interest for transistor devices but also for optoelectronic components for which a perfect alignment should be ensured between the input/output optical beam and the electrical addressing paths.

In 1995 Krauss et al. [3] proposed some possible self-aligned processes for ring lasers passivation and metallization. One of them, quite similar to our work consists in a double-layer composed of resist and metal for successively enabling the dry etch of the mesa and the passivation layer deposition. Compared to these previous processes, we further push forward the multiple use of one lithography step, by performing three successive and self-aligned key process steps, for the complete fabrication of VCSEL devices. We actually used a double photoresist layer definable with only one exposure and employing it for the remainder of the VCSEL fabrication processing steps: the etch mask for the mesa definition by ICP-RIE, the dielectric lift-off for the sidewalls passivation, and finally for metal contact lift-off. This process greatly simplifies the flow sequence and thus increases the reliability of the devices fabrication.

The process flow, which will be described more in details in the next section, is based on a self-aligned sequence of 8 intermediate steps including two lift-off steps and is described in Fig. 1. The first step consists in the double-layer resist spin coating, the bottom one (LOR30B), is optically transparent and used to form the undercut profile while the top one (SPR700) is a photosensitive resist used to define the effective device area. Then, during the second step, patterns are defined by exposing the top resist (405 nm), and a controlled development step to obtain the desired undercut profile. The resulting T-shaped structure is then used as an etching mask for to define the mesa by ICP-RIE. Subsequently, the SiO_x passivation layer is deposited by ICP-PECVD at low temperature (100 °C). The SiO_2-covered SPR700 resist is then lifted off to open the access for metal deposition. Finally, Ti/Au (50 nm/200 nm) contact is evaporated; while the LOR layer, still presenting an undercut profile can be finally used for the last metal lift-off.

Scanning Electron Microscope –SEM– pictures between several steps are shown in Fig. 2. These pictures are taken from a sample tilted at 52° and after Focus Ion Beam cross-section cut to allow the observation of the resists and device profiles.

As a proof of concept of this new self-aligned process flow, 980 nm VCSEL devices were fabricated. For the sake of simplicity, and to demonstrate the feasibility of the whole VCSEL process within one lithography step, air post VCSEL geometry are chosen, without lateral oxidation. Nevertheless the lateral confinement by oxidation or ion implantation can be easily implemented by adding another lithography step in the process flow. The VCSEL structure is composed – from bottom to top – of a GaAs Si-doped substrate, a 30 periods N DBR, 3 InGaAs quantum wells and a 19 periods P DBR top, and a GaAs top contact layer.

In the following section we will describe and discuss in details each step of the process.

The process starts by spin-coating the LORB to a thickness of 2.7 μm, to enable the lift-off of sufficiently thick (typically up to 500 nm) layers, and the SPR700 photoresist to a thickness of 2.3 μm.

After photolithography and development – step 2 –, suitable T-shaped disks are obtained. We get an undercut recess of 4.9 μm necessary for the future lift off. This undercut recess can be adjusted by varying the development time and by modifying the LOR soft bake temperature: etch rate is divided by a factor 2 between 170 °C and 200 °C [16]–.

Our process drastically increases the undercut dimension with respect to [9] where maximum 1 μm wide undercut has been achieved due to limitation of the mechanical strength of the SPR and the strain induced by the dielectric layer.

In the specific device described here the undercut length is not an essential parameter but if we want to considerably decrease the mesa diameter, the undercut has to be reduced, too. VCSEL of 10 μm aperture can be easily fabricated using our method. If we want to decrease aperture diameter beyond 10 μm we have to decrease the undercut to 1 μm as well as to modify the dielectric deposition recipe to avoid any deposition on the SPR photoresist sidewalls that will prevent the lift-off. This procedure will not affect the metal deposition and its lift-off since it is only realized by the LOR resist.

Due to the over-development, mandatory to obtain the LOR under-etch, the SPR shows angled slope sidewalls, shape that will be transferred to the mesa sidewalls after dry etch. This mesa angled slope ensures conformal deposition of the passivation film and later on of the top-contact metal deposition.

Dry etch by ICP-RIE of the mesas across the top DBR is performed under Cl_2-based chemistry and is controlled by an *in-situ* laser reflectometry monitoring system. As shown in Fig. 2 – step 3, an etch depth of 3.3 μm has been aimed in order to stop the etching within the intrinsic active region. During this step, the SPR topmost photoresist layer is also etched but with a rate about three times slower than the AlGaAs semiconductor. After the mesa etch, the remaining thickness for the SPR photoresist is 1.1 μm, which is sufficient to achieve the subsequent SiO_x passivation lift-off. Furthermore, this plasma etch also reduces the LOR undercut recess from 4.9 to 2.6 μm, a size which remains sufficient for next lift-off steps.

As depicted in Fig. 2, after the step 4, a Pt thin layer is locally deposited with the FIB ionic column system (appearing in grey on top of the mesa); this metallic layer does not play any role in the VCSEL process, but is used to increase the contrast of the SEM images and thus to measure more easily the SiO_x and SPR thicknesses. The maximum thickness of the SiO_x that can be deposited is, strictly speaking, limited by the initial LOR resist thickness, but, in reality, the SPR could break-off under the accumulated strain of the thick SiO_x layer. For this reason, a post exposure bake (PEB) is applied to harden the photoresist layer, while the ICP-PECVD deposition has to be