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Physical, chemical and electrical characterisation of the diffusion of copper in silicon dioxide and prevention via a CuAl alloy barrier layer system

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ABSTRACT

Cu and CuAl alloy (90%:10% wt) films deposited on thermally grown SiO_2 were studied using thermal stress testing in vacuum, N_2 flow and atmosphere ambient all at a temperature of 500 °C, in order to rigorously test the effectiveness of the incorporation of Al into a Cu film at preventing degradation of the metal layer and diffusion of Cu into the underlying SiO_2 dielectric. Capacitance voltage testing of metal-oxide-semiconductor (MOS) devices, using the Cu and the CuAl alloy as the gate metal show the failure of the Cu reference set via diffusion of Cu at the metal / SiO_2 interface in contrast to the stability of the CuAl alloy devices, even following a 500 °C anneal in atmosphere ambient. The flatband voltage of the Cu reference MOS structures were altered by the application of an external applied voltage bias, consistent with the diffusion and mobility of Cu^+ ions into the underlying SiO_2 layer. Optical and scanning electron microscopies of the surface metal layers show the degradation and delamination of the pure Cu films throughout the experimental anneal stages, in contrast to the stability of the CuAl alloy. X-ray photoelectron spectroscopy shows the growth of Al oxide at the surface of the CuAl alloy following thermal anneal which acts to passivate the film, preventing Cu oxide formation which was identified in the pure Cu reference sample set. Transmission electron microscopy analysis shows the inter-diffusion of Cu at the Cu / SiO_2 interface following anneal, in contrast to the CuAl alloy which shows the growth of a continuous barrier layer interface. Time-of-flight secondary ion mass spectroscopy (ToF-SIMS) was used to profile the entire metal / SiO_2 / Si stack via 3 dimensional reconstructions, showing the inward diffusion of Cu within the Cu control samples and containment of Cu within the metal layer of the CuAl alloy samples.

1. Introduction

Moore's law continues to be upheld as device geometries in IC fabrication continue to shrink. Challenges due to the shrinking of on-chip devices arise in the areas of materials, materials growth and characterisation [1]. With the change from aluminium (Al) to copper (Cu) as the interconnect material of choice in back end of line fabrication for high speed integrated circuits, a number of benefits were realised, including increased conductivity, decreased power consumption and increased resistance to electromigration failure [2,3]. However, there are a number of issues which accompany the introduction of Cu interconnects, most notably the poor adhesion to any Si based inter-layer dielectric (ILD) material and diffusion of Cu into the surrounding ILD materials [4–7]. The diffusion of Cu from the interconnect line into the surrounding ILD or device active regions cannot be tolerated due to the fact that Cu can create deep level traps in Si, degrading device performance and ultimately rendering them dysfunctional [7]. In order to constrain the Cu within the conducting line, a physical barrier composed of Ta/TaN is typically used [8,9]. As interconnect lines shrink with continued device scaling, the barrier layer must also reduce in dimensions in order to allow maximum volume within the interconnect line available for Cu metallisation. Self-forming barriers have emerged as a possible candidate to replace the discretely deposited Ta/TaN barrier system [10–13]. In order to create a self-forming barrier, a metal is alloyed with Cu in the conducting line or seed layer. Post metallisation annealing then causes the alloying element to be expelled from the interconnect line towards all interfaces, including the metal / ILD interface [14]. Ideally, as the alloying

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element reaches the ILD interface, it chemically reacts with the top few nanometres of the ILD in a self-limiting fashion (1–2 nm) in order to form a metal oxide or metal silicate barrier [15–17]. This self-forming barrier must satisfy a number of criteria including (a) adhesion promotion of the interconnect line to the ILD surfaces, (b) prevent any Cu diffusion from the metal line into any surrounding ILD material and (c) passivate the interconnect line in order to reduce damage during thermal processes. Aluminium has emerged as a possible element to alloy with Cu in the metal line in order to form a self-forming barrier due to the thermodynamic stability of Al in forming metal oxide species [18–20].

2. Experimental details

Metal oxide semiconductor structures were fabricated on n-type (100) Si wafers (P-doped with the resistivity of 2–4 Ω.cm) which had 120 nm of thermally grown SiO_2 on the surface. Metal gate areas of 2 mm×2 mm, 1 mm×1 mm and 200 μm ×200 μm were defined on the surface of the SiO_2 by lift-off lithography, with both Cu and CuAl (90:10% wt) alloy gates sputter deposited from dedicated sputter targets to a thickness of 250 nm in order to create MOS structures which differed only by the addition of 10 wt% Al in the alloy gate samples.

Multi-frequency (1 MHz and 10 kHz) capacitance voltage (CV) sweeps were performed on an Agilent B1500 semiconductor device analyser in conjunction with a Cascade probe station system in order to identify any device failure associated with the diffusion of Cu^+ ions at the metal / SiO_2 interface. All CV sweeps were performed following a +10 V hold (on the metal gate contact) for 300 s in order to bias any mobile Cu^+ ions in the dielectric material towards the Si/SiO_2 interface (unless otherwise stated), thus allowing any flatband voltage shifts due to the presence of diffused Cu^+ ions to be detected. Hysteresis within the CV profile was tracked by recording a reverse CV sweep immediately following the initial forward bias sweep. Multiple devices across each sample set were tested (> 10); however, for clarity, only the representative results from a single device for each sample set are shown due to the high levels of reproducibility across each sample set. CV traces were measured using a 25 mV AC signal and ranged from +10 V to − 10 V (forward trace) and in a reverse trace following any negative biasing performed on the metal gates. Voltage steps for each CV measurement were 100 mV with a dwell time of 250 ms per data point.

All MOS devices received a post metallisation anneal in vacuum (at a pressure lower than 1×10^{-6} mbar) in order to remove sputter damage during fabrication and also to promote segregation of Al from the CuAl alloy sample to create a self-forming barrier at the metal / SiO_2 interface, unless otherwise stated. Thermal stressing of the devices was performed in a tube furnace within a class 1000 clean room at a temperature of 500 °C under (a) N_2 flow (5 l/min) in order to anneal in a reduced oxygen environment and (b) atmosphere ambient for 1 h. The calculation of the concentration of diffused of Cu^+ ions following the N_2 anneal stage was performed relative to the vacuum anneal stage of the same structure due to the electrical stability of the devices following vacuum anneal.

Four point probe analysis of blanket metal films was carried out using a Jandel Rm3-AR four point probe system in order to track the change in resistance of the metal layers following various ambient anneals.

X-ray photoelectron spectroscopy (XPS) analysis was carried out in an ultra-high vacuum (UHV) system at a base pressure of 1×10^{-9} mbar in order to examine the chemical state of the top most surface of the metal films. The photoelectrons were excited using a conventional Al Kα (hυ =1486.6 eV) X-ray source and analysed using a VG Microtech electron energy analyser operating at 20 eV pass energy yielding an overall resolution of 1.2 eV. Curve fitting analysis of the recorded core level spectra were fitted using Voigt profiles composed of Gaussian and Lorentzian line shapes using a Shirley-Sherwood background. All spectra were fitted concurrently with the various parameters fixed (not including the binding energy position of the Al oxide peak) to ensure consistency across the fitted spectra. Peak fitting analysis was carried out using AAnalyzer peak fitting software.

Transmission electron microscopy (TEM) was performed on a JEOL 2100 electron microscope operating at 200 kV in order to study the metal / SiO_2 interface of the annealed structures. TEM samples were prepared by a FEI Helios Nanolab focused ion beam, to prepare electron transparent, sub 100 nm thick lamella structures.

Time-of-flight secondary ion mass spectroscopy (ToF-SIMS) analysis was carried out in an ultra-high vacuum time-of-flight secondary ion mass spectrometry (TOF-SIMS IV) instrument (ION-TOF GmbH, Muenster, Germany) operating in non-interlaced mode, using a 25 keV Bi^{3+} ion analysis beam with a sputter current of 0.1 pA and a 10 keV Cs ion sputter beam with a sputter current of 30 nA, with a cycle time of 100 μs. Surface charging was compensated using a 20 eV electron flood gun. An area of 400 μm×400 μm was sputtered with the Cs ion beam during depth profiling, with analysis carried out by randomly rastering the Bi^{3+} ion beam in a 150 μm x 150 μm region in the centre of the sputter crater. The sputter and analysis cycles are interleaved at regular intervals during the sputter process to create a 3-D representation of the data. Depth profile thicknesses were calibrated by sputtering a deposited copper metal layer of known thickness. Copper metal is detected by tracking the Cu_3^- ion signal, with AlO_2^-, CuO^-, SiO_3^-, Si_3^- ion signals used to detect aluminium oxide, copper oxide, and the silicon substrate respectively.

3. Results & discussion

Fig. 1 displays 1 MHz CV profiles of a Cu MOS device following the various anneal stages of vacuum, N_2 flow and atmosphere, all at 500 °C. As can be seen following the vacuum anneal stage, the device appears to behave like an ideal MOS capacitor [21] with clear accumulation, depletion and inversion regions with no hysteresis present. Following the N_2 anneal, a negative flatband voltage shift is evident in addition to the observation of hysteresis in the CV profile, consistent with the diffusion of Cu^+ ions into the underlying oxide layer of the device, as reported in previous studies of CV analysis of Cu MOS devices [5–7,22,23,29]. In addition to the above changes, the slope of the CV profile in the transition region between depletion and inversion regions of the profile is reduced, which could indicate the possible presence of interface states at the SiO_2/Si interface. The mobile ion charge concentration N_m was estimated from the CV flatband capacitance (C_{fb}) as $N_m=C_{ox}\times\Delta V_{fb}/A\times q$, (assuming all charge is located at the metal / SiO_2) interface, where C_{ox} is the oxide capacitance, ΔV_{fb} is gate voltage difference at flatband capacitance between N_2 and vacuum

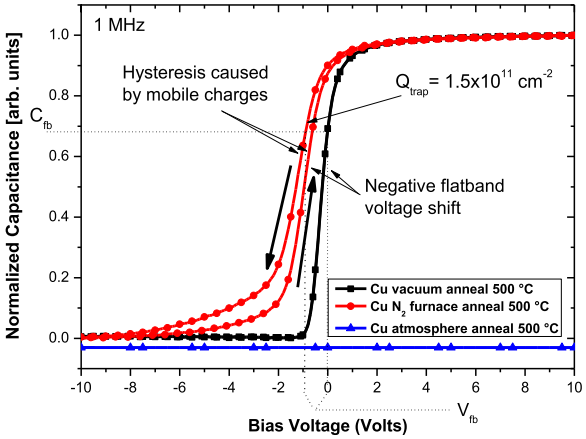

Fig. 1. CV plots of a Cu MOS device following 500 °C vacuum, N_2 flow and atmosphere ambient anneals indicating the electrical failure of the device.