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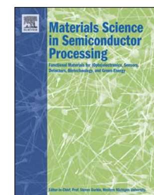

Doping of semiconductor devices by Laser Thermal Annealing

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ABSTRACT

In today's highly competitive semiconductor industry, and due to the accelerating pace of technology development, the integration of new and disruptive solutions to address process limitations is a mandatory requirement, although most challenging, Doping, i.e. the ability to control material properties locally and by extension local strain engineering, are amongst the key process variables used to overcome device performance issues. With the emergence of three-dimensional (3D) devices and architectures at the nanoscale, new doping schemes which rely on low thermal budgets are being evaluated, especially in the framework of new materials introduction such as germanium (Ge) and III-Vs in front end logic, defect engineered oxides and phase change materials in memory, or silicon carbide (SiC) and gallium nitride (GaN) in power devices.

Ultrafast sub-µs annealing schemes with shallow penetration depths providing localized impact, such as Laser Thermal Anneal (LTA), are some of the most promising and scalable approaches being evaluated today. Its production worthiness is already established as process of record for high volume manufacturing of several 3D stacked architectures such as vertical silicon (Si) and SiC power devices and complementary-metal-oxide-semiconductor (CMOS) imaging sensors.

This paper reviews recent work highlighting the potential of LTA as an enabler for next generation technologies covering a wide range of applications from Logic to Nano-Electro-Mechanical Systems (NEMS) and 3D sequential integration.

1. Introduction

The challenges for doping in recent technologies are mainly driven by the advent of three-dimensional (3D) oriented devices and architectures, coupled with the introduction of new materials, in response to the ever growing difficulty of scaling issues. Amongst these challenges, those addressed by low thermal budget anneal requirements are essentially diffusion control, interface and layer defectivity, doping conformity and buried layer integrity. The proper choice of anneal methods and parameters has a decisive impact on both device performance and overall yield. Sub-µs pulsed ultra-violet (UV) laser approaches such as Laser Thermal Anneal (LTA) are considered as serious candidates to help solve these foreseen manufacturing issues.

After a short summary of the specifics of the Laser anneal system (SCREEN LT series) considered for this review, we will cover its applications in 3 main areas: Logic including Silicon (Si), Silicon-Germanium (SiGe) and Germanium (Ge) materials; 3D monolithic integration including logic and internet of things devices; and, finally power devices including traditional Si and wide bandgap materials.

2. SCREEN LT Laser anneal system

SCREEN LT pulsed UV laser annealing technology (also named LTA) has already been described extensively in previous papers [1]. From a process perspective, the main features are its step-and-repeat anneal scheme (schematized in Fig. 1, left), the UV wavelength enabling shallow thermal diffusion length and the sub-µs to µs time-scale of the high temperature achievable near surface (up to melting point) thanks to its relatively short pulse duration (160 ns). From a manufacturing perspective, the latest system, called LT-3100, has additional capabilities useful for process tuning and optimization such as assisted heating (up to 450 °C), low oxygen ambient (< 10 ppm O_2) and a uniform anneal area adjustable up to stepper field size (< ± 4% beam non-uniformity over 26 mm×33 mm, as shown on Fig. 1, right).

The physics of this Laser annealing process in Silicon, including dopant and defect dynamics, have been studied extensively, both experimentally and theoretically ([2-5] and references therein), and have been implemented in a major commercial TCAD software tool [6,7].

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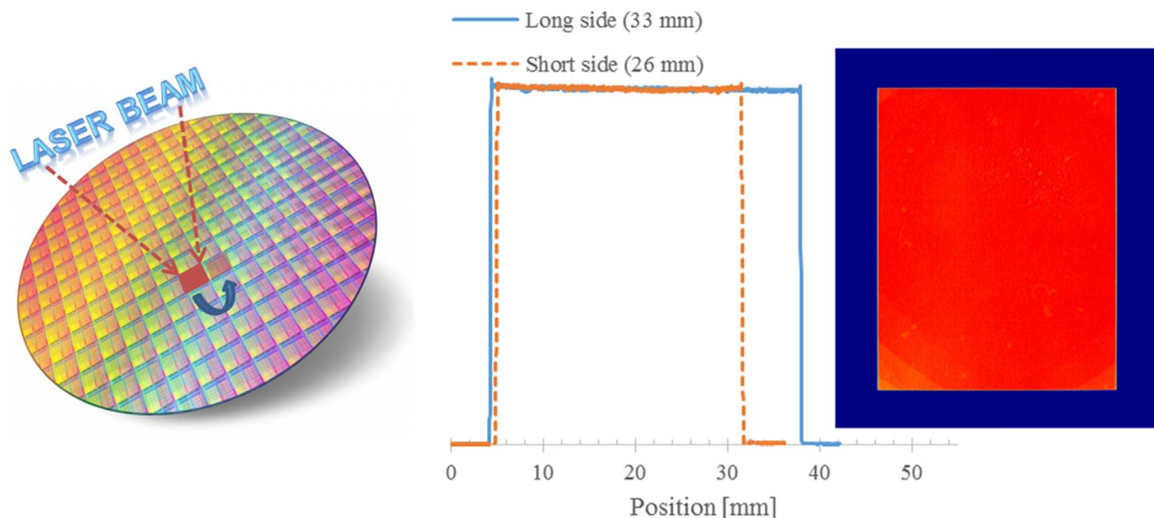

Fig. 1. (left) illustration of the step-and-repeat anneal scheme, (right) typical beam intensity profiles in X and Y direction and 2D intensity map (beam non-uniformity < ±4% over 26 mm×33 mm area).

3. Laser anneal for logic applications

A typical example of a logic fin field-effect-transistor (finFET) process flow is schematized on Fig. 2 (inspired by a shallow-trench-isolation (STI) -last finFET manufacturing flow [8]), highlighting key modules with high potential for the introduction of sub-µs laser annealing. In this section, we will specifically detail recent work for active area formation and Source/Drain (S/D) activation in Si and Ge applications.

3.1. Active area formation

The use of localized high mobility channel materials (such as SiGe or Germanium-Tin (GeSn) [9]) is one of the potential performance boosters for future complementary-metal-oxide-semiconductor (CMOS) technology nodes. Traditionally, such layers are obtained using selective epitaxy, with interface defects and surface roughness issues. The concept of active area formation by melt laser annealing is schematized on Fig. 3 for local SiGe formation (resp. GeSn) on epi-Si (resp. epi-Ge) using Ge (resp. Tin (Sn)) implantation followed by laser anneal in melting regime, where only the implanted region is addressed. Starting from a Si or Ge epi layer, such an approach would allow one to perform local strain engineering on the scale of the active layer.

Selective anneal is illustrated by the work reported in [10,11].

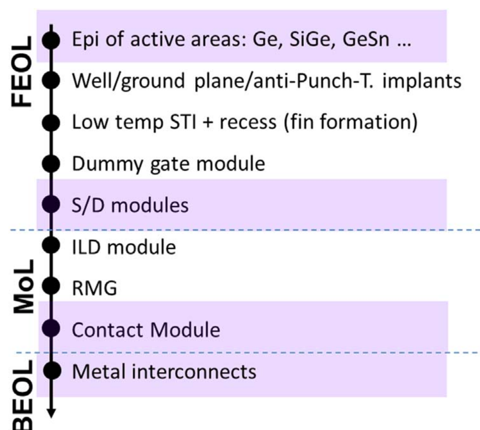

Fig. 2. Simplified STI-last finFET process flow (inspired from [8]) highlighting key modules where UV laser annealing has high potential.

Targeting SiGe layer formation, Si wafers were plasma implanted with very high dose germanium tetra-hydride (GeH_4) (3 kV, 1e17 at/cm^2) and di-borane (B_2H_6) (0.5 kV, 4e15 or 4e16 at/cm^2) then laser annealed. Fig. 4 shows the resulting melt depths extracted from secondary ion mass spectroscopy (SIMS) as a function of Laser energy density (ED, in J/cm^2) for Si with and without high dose Ge implantation. It appears clearly that the melting threshold for Ge implanted Si (<0.25 J/cm^2) is much lower than the pure Si case (1.7 J/cm^2). This can be explained by the lower surface melting temperature and the lower reflectivity (better coupling of the laser light) of the implanted region compared to the non-implanted one, in this case similar to the difference between amorphous and crystalline Si. Using proper laser conditions, cross-sectional transmission electron microscopy (TEM) reported in Fig. 5 shows a perfectly crystalline resulting SiGe layer and X-Ray Diffraction (XRD) shows a slight strain-induced peak shift, confirmed by differential Hall mobility measurements. To illustrate the scalability of the concept to new materials, a similar study has been done using Sn implantation in Ge [12]. 70 nm thick undoped Ge epilayers with SiGe buffer have been implanted with Sn (10 keV, 5e15 at/cm^2) then antimony (Sb) (11 keV, 5e15 at/cm^2) and laser annealed. Fig. 6 shows the resulting Sn SIMS profiles in Ge for non-annealed, non-melt, shallow melt and “deep” melt conditions. In the non-melt regime, no significant diffusion is observed. In the melt regime, Sn segregates near the surface above the solid phase solubility limit. XRD and differential Hall mobility results (not shown) suggest that Sn is properly incorporated, inducing strain and mobility improvement near the surface; however, more work is needed to fully understand the physics of strain formation in such a complex system.

The proof of concept for active area formation for channel material engineering by laser annealing has been demonstrated. The high incorporation rate restricted to a shallow depth can be obtained in the melting regime with optimized implant conditions. Selectivity and high incorporation rate are enabled by the shallow absorption depth of the UV irradiation, its short timescale and proper material engineering (here using implantation). The resulting strained layer may be considered as transistor channel or channel stressor similarly to the strained relaxed buffer approach [13,14]. The next step after optimization of the flow parameters (especially implantation conditions) is to validate the concept on electrical device structures.

3.2. Source/Drain doping

In today's and future CMOS technology nodes, the critical dimension of the contact at the transistor S/D has been scaled to below

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