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Review

Reprint of: N-type Doping Strategies for InGaAs☆

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ABSTRACT

Significant research effort has been placed into the use of III–V compound semiconductors, including InGaAs as channel materials in CMOS logic devices due to their superior electron mobilities compared to Si and other more conventional semiconductor materials. One of the major factors preventing industrial adoption of InGaAs as a channel material involves the minimization of source and drain contact resistances. To understand challenges to minimization of contact resistance, this work will outline the effectiveness of several doping approaches that have been attempted for n-type InGaAs including the use of silicon as a dopant and the effectiveness of each approach in achieving the highest level of activation possible. Previous and recently reported dopant diffusion behaviors are also included and discussed.

1. Introduction

There is continued interest in developing CMOS logic devices with channel materials that allow for faster transistor switching, lower power consumption, and improved heat dissipation than their silicon counterparts. III–V semiconductors, including the ternary alloy $In_xGa_{1-x}As$, are currently prime candidates for transistor channel materials due to their superior electron mobilities and injection velocities [1], and are currently included in the ITRS 2.0 roadmap [2]. For this review, the alloy composition lattice-matched to InP ($In_{0.53}Ga_{0.47}As$), will be referred to as "InGaAs," unless specifically mentioned. Due to their superior characteristics, III–Vs such as InGaAs will likely be used as a channel material for NMOS transistors, in conjunction with Ge or SiGe based PMOS transistors integrated onto a silicon substrate as demonstrated by multiple groups [3,4].

The need for lower contact resistances is of great importance, since its relative contribution to total device resistance increases with continued device scaling. A source and drain resistivity of less than 15 Ω-μm and 1 Ω-μm^2 are required to continue current ITRS scaling trends [5]. To attain these goals, maximizing activation of n-type dopants including Si is a major focus of research. This review discusses the n-type activation challenges of InGaAs and closely related materials as well as strategies to mitigate these limitations. Dopant diffusion behavior is also discussed, as predominant dopants have been recently observed to diffuse significantly during activating anneals.

2. Processing techniques

2.1. Annealing strategies

Annealing of III–V arsenides is one of the most obvious challenges of processing III–V materials. Group V species tend to evaporate leaving an excess of group III atoms resulting in loss of stoichiometry and degradation of the surface [6,7]. Group V overpressure, proximity capping, and dielectric capping have all been used to prevent the preferential evaporation of group V species [8–12]. Past research suggests that dielectric capping is the most successful method and recent advances with atomic layer deposition have allowed for the creation of thin, dense, and uniform dielectric capping layers to be deposited. Thin capping films better accommodate stress and limit cracks in the encapsulant from mismatches in thermal expansion between the substrate and capping layers. Dense films prevent out-diffusion through pinhole film defects [7]. It is also desirable in most cases to choose capping layers that can be selectively etched and removed from the sample substrate after annealing. Use of a 15 nm Al_2O_3 cap has been demonstrated as an adequate method to protect the surface of InGaAs and related materials [13–15]. Long-term anneals can also lead to growth of non-stoichiometric oxides, which can be

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mitigated by annealing under an inert gas ambient.

2.2. Material growth conditions

Growth conditions by MBE or Metal-Organic Chemical Vapor Deposition (MOCVD) have great impact on the material quality and abundance of specific point defects in InGaAs. One method used to influence the relative amount of point defects in III–Vs is by having either an As or Ga overpressure during growth. Since having Si occupancy on cation sites is preferred for n-type doping, growing III–Vs such as GaAs and InGaAs with an As overpressure will lower the amount of anion vacancies present in the as-grown material [16] and influence the amount of cation defects that would impact Si diffusion and activation. Arsenic overpressure is also a central parameter that is accounted for in several DFT and other calculations as a basis for the relative abundance of point defects present in a material [16–19].

2.3. Doping methods

A multitude of viable techniques exist to precisely control the doping concentrations in III–V arsenides. Bulk doping of unary and binary semiconductor crystals is often performed during growth from the liquid phase using the Czochralski, liquid encapsulated Czochralski, or Bridgeman growth techniques since they have congruent melting points. Ternary semiconductor systems generally do not have congruent melting points and therefore must be grown via CVD or MBE. Ion implantation has also been a historically useful technique for VLSI processes since it can be self-aligned by lithography features. The earliest doping techniques used an n- or p-type dopant gas or spin-on glass sources that drove the dopant into the bulk of the material by diffusion. Monolayer doping (MLD) is a newer iteration of this process that involves covalently bonding an organic dopant containing molecule onto the surface from a solution before driving the dopant into the bulk with an anneal. The advantages and disadvantages of these doping techniques are discussed for InGaAs in the subsequent sections.

2.4. Ion implantation

In ion implantation, dopants are ionized and subsequently accelerated by an electrical potential into the substrate material. The energy and dose of an implant are used to control the depth and concentration respectively of the dopant species in the host substrate. This process is highly energetic with the incident ions often travelling at large fractions of the speed of light. As a result, unlike other techniques, ion implantation results in a large amount of damage ranging from point defects to amorphization at high doses [20].

Ion implantation requires thermal annealing to recover damage and move dopant atoms onto lattice sites. In InGaAs annealing temperatures >550 °C are generally required to anneal damage and activate dopants but there is no indication that annealing temperatures greater than 750 °C improve dopant solubility in these materials [14]. Heated implants have been performed to limit the accumulation of damage during implantation and prevent the formation of amorphous layers in InGaAs at temperatures as low as 80 °C. One side effect of elevated temperature implants into InGaAs can lead to significant dopant channeling, leading to dopant profiles several nanometers deeper for heated implants compared to similar room temperature implants. Electrical activation of dopants implanted at intermediate temperatures (80–100 °C) is improved at short anneal times but prevention of amorphous layer formation in InGaAs is especially important since regrowth of III–V materials is especially disordered relative to Si [14,21–23]. This problem is exacerbated in the regrowth of 3-D structures as has been shown in Si and Ge [24,25]. While growth techniques report electrically active doping concretions of 3×10^{19} cm^{-3} or greater, ion implantation activation saturates around 1.5×10^{19} cm^{-3} [26].

2.5. Growth doping

Epitaxially grown doped layers of InGaAs with CVD or MBE regularly results in the highest n-type and p-type doping concentrations in InGaAs and other III–V materials. This seems to be due in large part to the ability to perform growth at temperatures much below the melting temperature of the solid, creating non-equilibrium doping conditions. The process of growing films by MBE is dominated by the surface incorporation kinetics of the precursors rather than towards equilibrium values, which can result in metastable films. A survey of growth doping literature indicates that lower growth temperatures generally result in higher n-type dopant activation [27–33] but some experiments indicate that exceeding the growth temperature during subsequent thermal treatments will result in deactivation in heavily doped substrates. This is likely to occur due to dopant-vacancy complexing [26,34,35]. Grown-in doping has a distinct advantage over ion implantation or monolayer doping as it does not require additional annealing steps for dopant incorporation or damage recovery. Multiple studies have shown that high carrier concentrations are often metastable beyond n-type doping concentrations of 1.5×10^{19} cm^{-3} after subsequent thermal anneals [26,29].

2.6. Monolayer doping

Monolayer doping more closely emulates the solid source doping method of the past. In this case, the amount of dopants that can be driven into the bulk are limited by the number of molecules that can be bonded to the surface. It has the potential to create damage-free junctions that are more abrupt than junctions formed with very low energy ion implantation. However, monolayer doping still requires the use of equilibrium diffusion to move dopants into the bulk [36–39]. There is no convincing evidence that monolayer doping provides better electrical activation of n-type dopants than what is observed in ion implantation since it is also limited by dopant-vacancy complexing. Conformal doping of 3-D structures such as fins and nanowires is likely the biggest advantage of monolayer techniques over ion implantation which suffers from shadowing effects.

3. Dopant selection and activation

Doping in the III–V family of materials is more varied than in elemental semiconductors since group VI and some group IV dopants behave as n-type dopants in InGaAs. Electrical solubility is one important factor in n-type dopant selection but diffusion behavior is also important to understand in order to develop effective processes for device creation. For sub-10 nm device formation it is generally desired to use dopants that can achieve high activation but also exhibit limited diffusivity.

3.1. N-type dopants

Group VI dopants such as S, Se, and Te are obvious choices for n-type dopants but are strongly differentiated by their diffusion characteristics in InGaAs. S is known to be a fast diffuser and likely proceeds by an interstitial mechanism which may complicate the creation of abrupt junctions in InGaAs while Se and Te have exhibited limited diffusion. Group IV species such as C, Si, Ge and Sn are often referred to as “amphoteric dopants” that can occupy either a group III or group V sublattice site. MBE experiments in GaAs provide the most convincing evidence that group IV dopants are amphoteric, as some experiments have demonstrated Si as both an n and p-type dopant. As the ratio of group III to group V flux can be modulated during growth, group IV dopants will preferentially occupy one site over another [40–44]. In practice, it is generally observed that these species are nominally n or p-type in III–V materials when introduced by ion implantation or source diffusion which rely on equilibrium thermal