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Modelling doping design in nanowire tunnel-FETs based on group-IV semiconductors

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ABSTRACT

The tunnel field-effect transistor (TFET), which utilises the band-to-band tunnelling mechanism for current conduction, provides the ability to achieve extremely low subthreshold swing (< 60 mV/dec) and very low off-current, thus offering a performance advantage over conventional inversion-mode metal-oxide-semiconductor field effect transistors (MOSFETs) for the ultra-low power and ultra-low voltage operation for the next generation of transistors. In particular, the optimisation of the TFET architecture and material composition is very important because the full potential of the TFET is not yet uncovered. In this work homo- and hetero-structure nanowire TFETs, based on Si, Ge and SiGe materials, have been investigated using device simulation, for the design of source and drain doping profiles, with nanowire diameters down to 5 nm.

1. Introduction

Over the years scaling-down of inversion-mode metal-oxide-semiconductor (MOS) field effect transistor (FETs) has delivered many advantages in integrated circuits such as high density circuits, high performance and reduced cost. However, the supply voltage (V_{DD}) has not scaled in proportion with device dimensions in order to keep high MOS drive current, leading to an increase in static power density in MOS integrated circuits. This is mainly due to a fundamental MOSFET limitation, which is the thermal limit of subthreshold swing (SS) of 60 mV/decade at room temperature. The result of V_{DD} scaling faster than the threshold voltage (V_T) is that the gate overdrive decreases, which in-turn negatively affects the on-state current (I_{ON}) and thus the device performance, such as the on-off current ratio (I_{ON}/I_{OFF}). Consequently, V_{DD} scaling has slowed down in order to maintain acceptable levels of gate overdrive. For example, assuming the ideal SS=60 mV/dec, if we shift V_T by 60 mV, this will lead to an increase of one decade of I_{OFF} in order to maintain the I_{ON} constant, which leads to a clear degradation of I_{ON}/I_{OFF} ratio, and an increase of static power consumption. Thus, alternative MOSFET device architectures are being investigated to mitigate this trend.

In a TFET, interband tunnelling is the basis of current conduction, and can be switched on and off quickly by controlling the band bending in the channel region. This conduction mechanism allows to obtain SS lower than 60 mV/dec, thus offering several potential benefits in analog and digital circuits [1–3]. However the TFET is an ambipolar device, showing p-type behaviour with dominant hole conduction and n-type behaviour with dominant electron conduction. By designing asymmetry in the doping profiles, or employing hetero-structures, the drain side tunnelling barrier can be widened to subdue the ambipolarity. According to the Wentzel-Kramers-Brillouin (WKB) approximation for tunnelling [4] the bandgap, the carrier effective mass, and the tunnelling screening length (λ) should be minimised for high barrier transparency. This is strongly influenced by several parameters, such as the device geometry, dimensions, doping profiles and gate capacitance [5].

The BTBT transistor device was first proposed in 1987 [6]. It took some time to realise as the first BTBT transistor to exhibit a subthreshold swings SS smaller than 60 mV/dec was experimentally demonstrated in 2004 via a carbon nanotube TFET [7]. III-V semiconductors have been studied as a potential material for TFETs, because III-V materials with small and direct bandgap offer advantages in achieving high tunnelling currents [8]. Nonetheless it is relatively difficult to integrate III-V semiconductors on a Si platform. Various TFET research works have been done using Ge [9–11], and SiGe [12–15].

In the homo-structure TFET, the source, channel and drain consist of the same semiconductor material. In a hetero-structure TFET different semiconductors are utilised in the source, channel and drain region. This may overcome some of the limitations of the homo-structure TFET. The concept of a hetero-structure TFET with an

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interface of two semiconductors with different bandgaps and band alignment offers the possibility of bandgap engineering for high I_{ON} while maintaining low I_{OFF} and suppressing ambipolar behaviour. Moreover, the narrower bandgap of a Ge and SiGe source region in the TFET helps to reduce the tunnelling distance and improves the subthreshold swing and I_{ON} current.

Recently a number of modelling-based studies have emerged in the area of group-IV based TFETs. Wang et al. did a simulation study of a GeSn/SiGeSn hetero-NTFET with a staggered tunnel junction [16]. The material compositions in the lattice-matched GeSn/SiGeSn were chosen to form band alignment at the hetero-interface. Ilatikhameneh et al. modelled nanowire based homo-structure TFETs to investigate if they can scale effectively below 10 nm [17]. A variety of channel materials were benchmarked, ranging from standard III-V semiconductors, to the more exotic WTe_2 and phosphorene. Sant and Schenk simulated band-offset engineering for GeSn-SiGeSn hetero TFETs, and explored variables including source doping, gate misalignment, material compositions and the effect of strain [18]. Min et al. presented an analytical model for the source doping effect in TFETs, and they observed that current peaks at a certain source doping level [19]. Verhulst et al. recently did a comparative analysis of n-channel and p-channel TFETs [20] and provided a perspective of TFETs for future low power technology [21]. Furthermore that group has many experimental TFET demonstrations [22], as well as an analysis of compressive and tensile strain effects in TFET devices [23,24].

In this work different homo- and hetero-structure nanowire TFETs, based on Si, Ge and SiGe materials, have been investigated using Sentaurus Technology Computer-Aided Design (TCAD) device simulation, for the design of source and drain doping profiles, with channel lengths approaching 10 nm and nanowire diameters down to 5 nm. Few works to date have focussed on nanowire-based TFETs, but the electrostatic control of a gate-all-around nanowire design may be required at these channel lengths. The goals for TFET optimisation are to simultaneously achieve the highest possible I_{ON}, the lowest average SS over many orders of magnitude of drain current, and the lowest possible I_{OFF}.

Note that the electric field at the source-channel region is crucial for TFET operation, and any variations in TFET design that alters this will have a large impact on device performance. This could also include gate alignment, spacer design, and contact schemes. These are all very important factors in TFET design, but here we will focus on the doping profile design within this paper.

2. Modelling SET-UP

The simulations have been carried out using the Synopsys Sentaurus TCAD software [25]. This involves computer simulation procedures to develop and understand 2D or 3D devices and probe their characteristics. The TCAD will give idealised results, however they give good insight into the physics and their impact on the tunnelling behaviour of the junction.

Band-to-band tunnelling (BTBT) is the most important model for TFET simulations. There is a choice to be made between local models, which use simple equations in which the electric field is an important parameter, and non-local models which have a more physical basis and don't depend on the electric field at the individual mesh points in the simulated device structure, but rather on band diagrams calculated along cross-sections through the device. The dynamic non-local BTBT model [26] has been used for all simulations in this work. The tunnelling path is assumed to start from the edge of the valence band and end at the edge of conduction band. Holes are generated at the starting point and electrons are generated at the end point which makes the tunnelling a non-local process.

Self-consistent device simulations have been performed with Sentaurus Device using the Fermi-Dirac statistics model, the drift-diffusion carrier transport, a doping dependent mobility model, the Auger and Shockley-Read-Hall generation/recombination models, the doping-dependent band-gap narrowing model, and the dynamic non-local path BTBT model at 300 K. In principle, all the qualitative trends are captured by the non-local BTBT model in Sentaurus TCAD, but the quantitative predictions are less reliable and need further calibration on experimental data or even new model developments. Furthermore in this work we use a semi-classical approach, a comparison between semi-classical and quantum-mechanical approaches can be found in the work of Vandenberghe et al. [27] For this reason, the qualitative trends presented here of TFET dependence on device design is expected to be correct, but the quantitative values should be handled with care.

3. Results and discussion

Unless otherwise specified, the source is highly doped p-type ($N_A=10^{20}$ cm^{-3}) and the drain is moderately doped n-type ($N_D=10^{18}$ cm^{-3}) respectively. The channel region is intrinsically doped. High-k material HfO_2 is used as the gate dielectric with an equivalent oxide thickness of 0.6 nm and the gate metal electrode work function is 4.2 eV in all the simulations. The supply voltage V_{DD} has been set to 0.5 V, which is reasonable considering the future application window for TFETs is expected to be at low supply voltages. Note the simple drift-diffusion model it is expected to underestimate the I_{ON} for channel lengths approaching the 10 nm. But this is not significant here because of the qualitative nature of this study. All the numerical simulations for homo- and hetero-structure nanowire TFETs have been obtained by considering the three-dimensional structure which is schematically presented in the inset of Fig. 1.

Three homo-structure TFETs were simulated, namely homogeneous Si, or Ge, or $Si_{0.5}Ge_{0.5}$. Two different hetero-structures have also been simulated, considering $Si_{0.5}Ge_{0.5}$ or Ge as a source region materials, with the rest of the structures comprised of Si. These TFETs are named “SiGe-Si” and “Ge-Si” respectively in this section. The bandgap in Si is assumed to be 1.1 eV, in Ge to be 0.66 eV, and in $Si_{0.5}Ge_{0.5}$ to be an intermediate value. Note in the hetero-structures, there may be strain introduced in the channel due to the difference in lattice constants between the 2 materials. As stated earlier Kao et al. performed an analysis of compressive and tensile strain effects in TFET devices.[23,24] It can be seen in those works that strain can have a large impact on drive current in TFETs. For simplicity strain effects are not

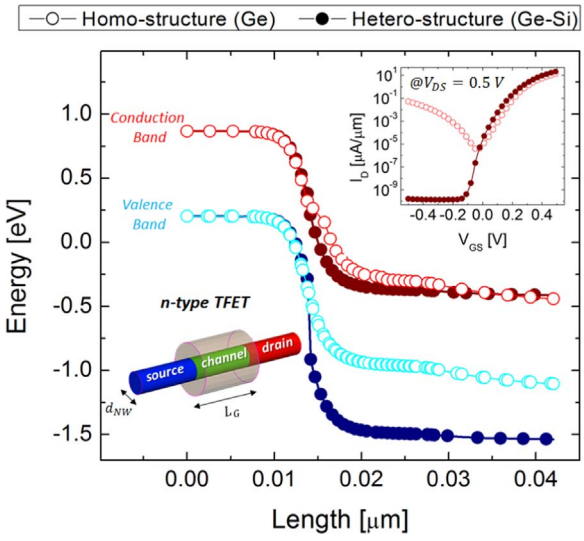

Fig. 1. Band diagram comparison of the Ge homo-structure and the Ge-Si hetero-structure TFETs in the on-state. The inset shows that all simulations for homo- and hetero-structure nanowire TFETs have been obtained by considering the 3D structure. Also in inset the I_D versus V_{GS} characteristics comparison of the Ge homo-structure and the Ge-Si hetero-structure TFETs for L_G =14 nm and d_{NW} =5 nm at V_{DS} =0.5 V.