Materials Science in Semiconductor Processing (xxxx) xxxx–xxxx

Contents lists available at ScienceDirect

Materials Science in Semiconductor Processing

journal homepage: www.elsevier.com/locate/mssp

Efficient defect identification of soft failures induced by device local mismatch for nano-scale SRAM yield improvement

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ARTICLE INFO

Keywords:
Device
Local mismatch
Fault isolation
Nano-probing
Test
SRAM

ABSTRACT

As the device size continues shrinking to nano-scale region, tiny defects induced device local mismatch in SRAM array becomes a major yield limiter. It is often quite time consuming and challenging to identify such kind of invisible defects through conventional FA techniques. This paper presents an efficient methodology on device local mismatch fault isolation with the combination of test features, advanced Electrical Failure Analysis (EFA) and Physical Failure Analysis (PFA) techniques. A successful case study involving this advanced methodology will be also discussed.

1. Introduction

SRAM memory is susceptible to process defects due to its high density, and it can be bitmapped to catch the failure location accurately, therefore it has been long recognized that SRAM is an ideal Technology Qualification Vehicle (TQV) for defect monitor and yield improvement during technology development [1–3].

The SRAM failure modes, as shown in Fig. 1, are categorized by the patterns of failure bit maps into world line cross bit line (WL X BL), bit line (BL), quad bit (QB), Double-Bit-Column (DBC), Double-Bit-Row (DBR), single bit (SB) and so on. It is obvious to find from Fig. 2 which shows the schematic of a six-transistor SRAM cell that among those failure modes SB issue [4,5] is the most challenging one to be found out the root cause for failure, because any defect occurred on any of the six transistors or interconnect will cause SB failure.

The fault isolation for most hard SB failures can be successfully fulfilled by combining the conventional FA techniques of Passive Voltage Contrast (PVC), Scanning Electron Microscope (SEM), Focused Ion Beam (FIB) and Transmission Electron Microscope (TEM). However, for the non-visible defect (NVD) such as device mismatch induced soft fail, fault isolation and defect identification cannot be achieved efficiently by mean of these conventional FA techniques only. Besides, in order to shorten the process development stage, there are plenty of PFA jobs have to be completed promptly to create a process defect Pareto chart. As shown in Fig. 3, this Pareto chart will help Technology Development (TD) team to rapidly focus on major issues and work out the solutions. Therefore, it is crucial to find out an analysis methodology to quickly and efficiently identify the root causes of such kind of non-visible defects [6–10]. This paper proposes an efficient analysis methodology combining advanced SRAM test features and fault isolation techniques to improve the cycle time of root cause identification, and also presents a case study which adopts this methodology to isolate a subtle defect successfully. This subtle defect, which is difficult to be isolated by conventional FA techniques, induces device local mismatch and finally causes SRAM SB soft fail.

2. Defect identification methodology for device local mismatch induced SRAM failure

Fig. 4(a) shows the traditional SRAM failure characterization flow, which basically is effective to identify the root causes of hard failure bits. In this flow, bit-mapping analysis is employed to indicate the failure address first, and then the conventional FA techniques are applied to analyze the failure root cause. In the case of conventional FA techniques, the first is using PVC to point out the abnormal contact position, followed by observing the defect that caused SRAM cell failed by means of the TEM lamella of failure location prepared by FIB. However, device local mismatch induced soft fail is usually difficult to be identified through the traditional SRAM fail characterization flow, since PVC and TEM image analysis for such kind of defect may not present anything abnormal. Consequently, it is classified as NVD and yield is suffered. The advanced SRAM failure characterization flow proposed in Fig. 4(b) is efficient to identify such kind of defect. The advanced failure characterization methodology in Fig. 4(b) screens out the most possible transistors suffered from device local mismatch issue, and then the enhanced FA techniques of nano-probing, Electron

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http://dx.doi.org/10.1016/j.mssp.2016.12.006
Received 5 July 2016; Received in revised form 30 November 2016; Accepted 2 December 2016

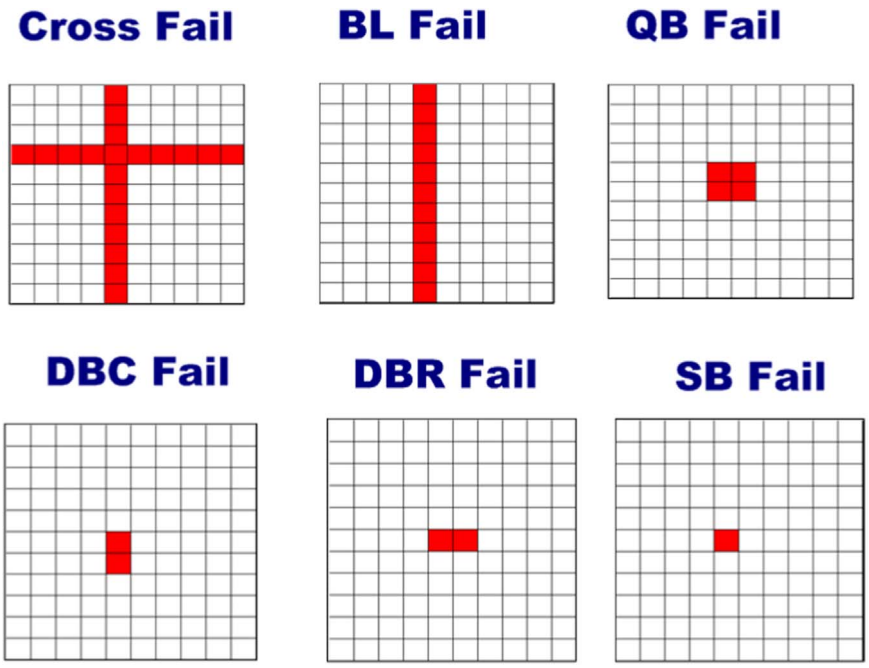

Fig. 1. Typical failure modes of SRAM. They are categorized by the patterns of failure bitmaps.

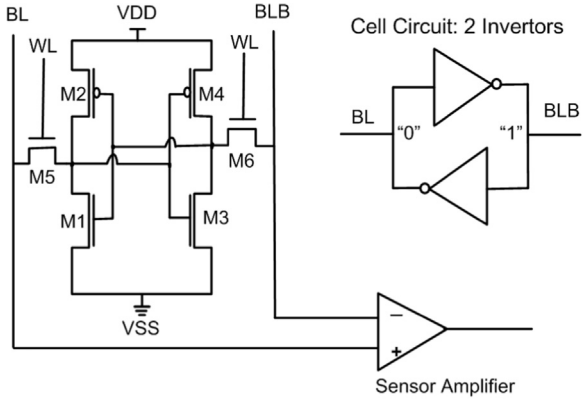

Fig. 2. Schematic of a six-transistor SRAM cell. An SRAM cell comprises two back-to-back connected inverters which form a latch and two access transistors. Access transistors serve for reading and writing access to the cell.

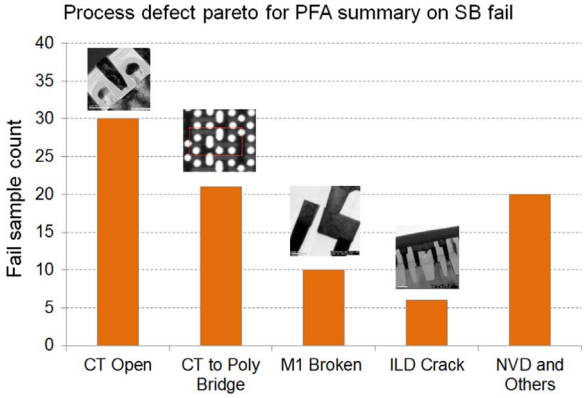

Fig. 3. Process defect Pareto chart. The physical root cause of non-visible defect (NVD) cannot be determined efficiently by conventional FA techniques.

Energy Loss Spectrometry (EELS) and junction stain techniques are applied to clarify the failure root cause.

2.1. Advanced failure characterization methodology

The characterization methodology consists of a special test pattern for SRAM fault model categorization and a special test feature for read current measurement of core cells. This methodology screens out the potential defective transistors from the six transistors of an SRAM cell. As a result, the FA success ratio and cycle time are improved significantly.

2.1.1. Special test pattern for SRAM fault model categorization

The conventional SRAM test pattern is shown in Fig. 5(a), which can only identify the failure chip location and failure bit address. Since one bit consists of six transistors, engineers still have to spend much time to analyze all of the 6 transistors. The special test pattern for SRAM fault model categorization is shown in Fig. 5(b). The hard failure units would be separated from the whole SRAM malfunction chips first in the special test pattern, and then conventional FA techniques could be applied directly for them to find out the failure root cause. In the following steps of the special test pattern, the soft fail units would be categorized as four types of failure: (1) Write Failure; (2) Read Failure; (3) Read Disturb Failure and (4) Data Retention Failure. Empirically, Read Disturb and Write failures dominate the failure rate of the soft failures. This is owing to that the SRAM cell must be sized as small as possible to achieve high memory density, whereas the smaller and denser the devices are, the more susceptible they are to process variation induced shift of critical parameters. The shift of critical parameters, such as threshold voltage (V_T), leakage, effective gate length or width will degrade the read stability and writability of SRAM cell operation, and eventually cause Read Disturb and Write failure [11–13].

An SRAM cell's read stability and writability can be determined by beta (β) and gamma (γ) ratio. They are shown as below:

$$\beta = Ion\_PD/Ion\_PG \quad (1)$$

$$\gamma = Ion\_PG/Ion\_PU \quad (2)$$