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EMBEDDED VERNIER TDC WITH SUB-NANO SECOND RESOLUTION USING FRACTIONAL-N PLL

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Abstract: A novel implementation technique for Vernier-based time-to-digital converters is reported. It is based on fractional-*N* phase-locked loops which allows the design of Vernier clocks with very close frequencies. The Vernier registers comparing counter values have been implemented in hardware in order to guarantee minimum detection latency of the moment of coincidence. Two Vernier clocks with close frequencies increment two 24-bit counters in a Cyclone V FPGA. A Vernier TDC with a demonstrated time resolution of 476 ps is reported. It is also established that the time resolution limit that can be achieved with the suggested design is 10 ps.

Keywords: time-to-digital converter, phase-locked loop, Vernier, FPGA, fractional-*N* PLL

INTRODUCTION

The ability to measure time accurately is a fundamental presumption in a number of scientific applications. High precision/high resolution time interval measurements are required in any instrument that relies on time-of-flight to extract the measurand such as mass spectrometers (Skoog & Leary, 1992), radars (Richards, 2014) and sonars (Waite, 2002).

The fundamental method to measure time in digital systems is to simply count pulses from a reference clock and the time resolution is limited by the reference clock's frequency which of course has a physical and practical limit. The difference between a basic counter and a TDC (time-to-digital converter) is the fact that a TDC can extract interpolated time values between the reference clock's edges (Henzler, 2010). This is either done using time stretching (Nutt, 1968) or Vernier clocks (Porat, 1973).

The Vernier clock principle is based on two competing clocks and the overall time resolution equals the difference in the two clocks' period (see Theory section). So far, few solutions based on this technique have been reported. The main reason for that is the lack of available clocks; in order to provide the necessary precision, they need to be crystal based and in order to provide the necessary resolution they need to be very close in frequency. Crystal pairs close enough in resonance frequency are simply not available. However, since fractional-*N* PLLs are now becoming available in integrated SoC (System-on-Chip) circuits, the Vernier clock TDC method can be directly synthesized in an FPGA (Field Programmable Gate Array). This work will present such a solution and demonstrate a time resolution of 476 ps with a < 5 ppm precision over a dynamic range of 24 bits.

Previous Vernier TDCs have mostly been synthesized by large arrays of FFs (Flip-Flops) and delay buffers where the leading edge of the time pulse sets the inputs to logic 1 in successive order, and each buffer has a delay t_D, and the trailing edge clocks the FFs (with a buffer delay $t_{clk} < t_D$), see figure 1. Since $t_{clk} < t_D$ the trailing edge will eventually catch up with the leading edge and only the FFs where the leading edge arrived before the trailing edge will be set; the Q outputs of the FFs represent a "temperature" value of the time interval.