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Basic metrological properties of electronic oscillators with direct digital synthesis

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ABSTRACT

Signal oscillators based on DDS (Direct Digital Synthesis) are widely used in recent years.

However, order metrological characteristics of signals generated by these oscillators have not been studied in many cases, and uses of such oscillators are not always justified. First of all, signals of the most popular sine waveform are unsatisfactory in terms of metrology, including errors of amplitude, period and their instability, total harmonic distortion.

Certainly, with the development of integrated circuit fabrication technology, errors of basic units decrease. Therefore, it can be expected that instrumental errors will be decreasing in the nearest future. However, not only instrumental but also method errors are intrinsic to direct digital synthesis of signals. These method errors will determine limiting metrological characteristics as a hardware component of digital oscillators continue to be improved.

When considering metrological characteristics of DDS-based digital oscillators, it is necessary to take into account that their output signals are quasiperiodic. This produces a complex spectrum of signals.

Three methods for estimating a spectrum are proposed. Summation of amplitudes of spectral components in modulus is found to determine the level of signal amplitude and its instability, while vector summation determines period and its instability. Finally, root mean square summation determines total harmonic distortion.

This paper analyzes limiting distortions of an output sine-wave signal with the aim of identifying the most appropriate application of these oscillators.

It should be noted that the method error in this case is a theoretical error, which is very difficult to determine experimentally against other errors. Therefore, only results of mathematical modeling are given in the article.

We present the graphics that allow right sampling frequency to be chosen depending on a specified error of amplitude, error of period, and total harmonic distortion of output voltage.

1. Introduction

Measuring signals in modern digital oscillators are often generated on the basis of the direct digital synthesis (DDS) technology. This technology makes it possible to reproduce signals of different waveforms, including traditional sine-wave, triangle, and square ones.

They have a number of advantages over analog oscillators. The principles of DDS operation are described in studies [1–6]. Spectra of signals at the output of industrial oscillators are experimentally studied in [7–10]. Different methods of distortion reduction are discussed in [6–10], in particular by connecting two oscillators in parallel [7,9] and introducing binary noise sources [5,10]. Spurious free dynamic range (SFDR) is considered in [4,5,17,18]. Different applications of DDS oscillators are discussed in the literature, e.g. music in [11], frequency synthesis in [14,15], and distortion measurement in [12,13]. Almost all of these issues are covered in the monograph [16]. However, none of these studies consider metrological characteristics of output signals in a systematic way. This study is aimed at calculating the most important metrological characteristics: amplitude, output voltage period, and instabilities thereof.

The DDS principle is unique due to the fact that a generated signal is synthesized with a high degree of accuracy that is typical to digital systems since frequency, amplitude and phase of a signal are exactly known at any time. The elements of DDS are almost not subject to temperature drift and ageing. Now, the integrated-

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circuit technology makes it possible to combine all DDS modules on a single chip. That is why, thanks to high technical and application performance, DDS signal oscillators are pushing out analog oscillators of the market.

However, metrological characteristics of signals generated by these oscillators often do not meet the current requirements. Signals of the most demanded sine waveform are especially unsatisfactory in terms of metrology, including total harmonic distortion, amplitude error, a period and phase instability [19,20].

Certainly, with the development of integrated circuit manufacturing technologies, DAC errors decrease, while digit capacity of adder accumulators increases. Consequently, instrumental error can be expected to decrease in the nearest future. However, not only instrumental, but also method errors are typical of direct digital synthesis of signals. These are method errors which remain to be limiting metrological characteristics while a hardware component of digital oscillators will be improved further. This article first analyzes basic metrological characteristics sine wave output of generators.

After the introduction, Section 2 describes the principle of DDS operation and shows that, in the general case, output signals of an oscillator are quasiperiodic. This causes a change in amplitude, period, and instabilities therefore, as well as gives rise to nonlinear distortion. Then, Section 3 discusses some methods of signal spectrum calculation for determining metrological characteristics of a signal: instability and distortion. In Sections 4–6, these parameters are calculated depending on a specified length of the output voltage period.

2. Basic principles of direct digital synthesis

In order to understand why method errors occur, let us recall the principle of signal generation based on direct digital synthesis. This principle is well known [1,3,4].

Signals are generated by oscillators through a continuous curve approximated by a sequence of adjacent square-wave pulses of different amplitudes and durations. In essence, waveform of output voltage is generated by time-sequential reproduction (summation) of these square-wave pulses of specified amplitude. This method fits well into the sequential summation method discussed in [2], being its special case.

The oscillator (see Fig. 1) is based on an adder accumulator (AA). The digital bit word N_f that determines frequency of an output signal comes to AA and, with clock frequency f_0, is added to the word M_f accumulated in it by that time. If the adder is overfilled, i.e. the number exceeds AA capacity (M), summation continues with the remaining part. Therefore, the current digital code M_f changes almost periodically according, to the linear law. Then, coming to look-up table (LuT), it serves as an address of a respective memory cell in which another number is stored. If values of a sine function are sequentially written in these cells, digital words which are proportional to the sine function will appear at the LuT output with frequency f_0.

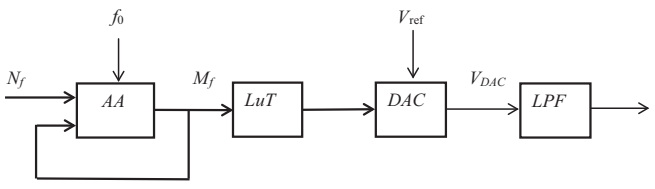

Fig. 1. Block diagram for implementation of the direct digital synthesis method: *AA* – adder accumulator; *LuT* – look-up table; *DAC* – digital-to analog converter; *LPF* – low pass filter.

The output voltage waveform after transformation of the code in *DAC* is composed of square-wave pulses of different amplitudes, which, is filtered *RC* or *LC* filter (*LPF*) and represent the output voltage.

In Fig. 2, the piecewise step growing curve in the oscillogram for generating a sine-wave signal shows the sequence of changing the number M_f in *AA* register. The output voltage waveform after transformation of the code in *DAC* is presented in the bottom part of the figure. Here, the *DAC* output voltage is composed of square-wave pulses of different amplitudes, which, as a whole, represent the output voltage. The dashed line shows the output voltage after filtration.

The voltage at the DAC output is seen (see Fig. 2) to be non-periodic since it is composed of quasiperiods containing different numbers of clock intervals. The output oscillation at each quasiperiod contains n or m clock intervals t_0 (periods of reference (clock) frequency). Note that these numbers differ by one. The first quasiperiod contains n intervals t_0, the second – m intervals, etc. The recurrent periodic process consisting of several quasiperiods of nt_0 and $(n+1)t_0$ can be observed for a long time.

The periodicity of the process can be defined by the following equation:

$$K\ nt_0 + L(n+1)t_0 = (K+L)T_{out}, \tag{1}$$

where K is the number of quasiperiods of nt_0, L is the number of quasiperiods of $(n+1)t_0$, T_{out} is the period of the output signal.

Taking into account that $T_{out} = 1/f_{out} = 1/f_T\ N_f/M = t_0\ M/N_f$,

$K\ nt_0 + L(n+1)t_0 = (K+L)T_{out} = (K+L)t_0M/N_f$. The left and right part of this expression can be reduced by t_0. Then, we obtain the invariant expression in relation to the clock interval.

$$K_n + L(n+1) = (K+L)M/N_f. \tag{2}$$

If the terms are combined with K and L on the left and right, we obtain the expression:

$$K(n - M/Nf) + L(n + 1 - M/N_f) = 0.$$

This equation belongs to Diophantine equations with unknown integral numbers K and L since all its values are integral numbers as well. It is understood that one equation with two unknown variables K and L may have many solutions in integral numbers. Let us rewrite the Eq. (1) as:

$$K = -L((n+1)t_0 - T + \text{out})/(nt_0 - T_{out}) \tag{3}$$

For example, at the required output voltage period $T_{out} = 6.5$ clock intervals, two quasiperiods of 6 and 7 clock intervals should be sequentially generated to ensure the average period of 6.5 intervals. This follows from the Eq. (3)

$$K = -L(6 + 1 - 6.5)/(6 - 6.5) \text{ or } K = L(0.5)/(0.5) = L.$$

Here, $K = L = 1$ or $K = L = 2$, etc. This oscillation will repeat every 13, 26, 39, etc. clock intervals.If oscillation with the period of 6.33 clock intervals is to be generated, this average period will be generated from the same quasiperiods with 6 and 7 intervals, since

$$K = -L(6 + 1 - 6.33)/(6 - 6.33) \text{ or } K/L = 0.67/0.33.$$

In this case, numbers K and L can take only integral values. Therefore, K and L should be taken equal to 67 and 33, respectively, so that the relations on the left and right are equal t_0 each other. This means that, at 33 quasiperiods each consisting of 7 intervals, DDS must generate another 67 quasiperiods each consisting of 6 intervals so that the average period is equal to 6.33 clock intervals. This oscillation will repeat every 633 clock intervals.

In a similar way, the output signal with any non-integral value of the period is generated. In this case, such a signal will be periodic after 10^k of clock frequency periods, where k is the number of digits after decimal point in a specified fractional part of the per-