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Planar junctionless phototransistor: A potential high-performance and low-cost device for optical-communications

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ABSTRACT

In this paper, a new junctionless optical controlled field effect transistor (*JL-OCFET*) and its comprehensive theoretical model is proposed to achieve high optical performance and low cost fabrication process. Exhaustive study of the device characteristics and comparison between the proposed junctionless design and the conventional inversion mode structure (*IM-OCFET*) for similar dimensions are performed. Our investigation reveals that the proposed design exhibits an outstanding capability to be an alternative to the *IM-OCFET* due to the high performance and the weak signal detection benefit offered by this design. Moreover, the developed analytical expressions are exploited to formulate the objective functions to optimize the device performance using Genetic Algorithms (*GAs*) approach. The optimized *JL-OCFET* not only demonstrates good performance in terms of derived drain current and responsivity, but also exhibits superior signal to noise ratio, low power consumption, high-sensitivity, high I_{ON}/I_{OFF} ratio and high-detectivity as compared to the conventional *IM-OCFET* counterpart. These characteristics make the optimized *JL-OCFET* potentially suitable for developing low cost and ultrasensitive photodetectors for high-performance and low cost inter-chips data communication applications.

1. Introduction

The resistive loss of the electric wire in inter-chip data communication originates electric signal attenuation and distortion, which imposes the use of signal processing to maximize the emitted information [1–3]. Recently, condensed efforts and attentions have been paid to optical interconnects due to the lower resistive losses and the enormous bandwidth achieved in optical wireless communication systems (*OWCS*) [4,5]. However, these systems consume a huge amount of power owing the high power dissipation of the optical receivers. In this context, several optical structures based on Schottky barrier photodiode, *MSM* photodetectors and *FET*-based phototransistors have been investigated during the last few years in order to improve the *OWCS* performance [6–13]. Obviously, the *FET*-based phototransistor is regarded as the most common device to open up the possibility for avoiding the high density of the optoelectronic readout circuits. To this extent, scientific endeavors demonstrate a great interest to the *Ge*-based *OCFET* owing the new epitaxial techniques for growing the *Ge* on silicon platform [12,13]. Unfortunately, the *Ge*-based *OCFET* operating at $\lambda = 1.55$ μm has revealed excellent performance but only with individual tenability that is, low power and cost devices or high performance and ultrasensitive phototransistors. Moreover, the use of highly doped *Ge* gate can exacerbate the dark current and hence degrade enormously the device *FoMs*. Evidently, it is of great significance to explore how to overcome the trade-off between the low fabrication cost and ultrasensitive devices. Therefore, new approaches and design methodologies should be developed in order to improve the *OCFET* regarding these aspects. For this purpose, it is important to originate lower cost structures as well as improving the optical and the electrical behavior of the conventional *Ge-OCFET*. In this context, the Junctionless (*JL*) design can open up the route not only for reaching the reduced fabrication cost but also for achieving ultra-sensitive devices. In this perspective, the main advantage offered by this design resides principally in avoiding the elaboration of the *S*/*D* regions (n^{++}) and hence the establishment of junctions that seems to be not a trivial task. This constitutes a serious problem that imposes the high fabrication cost for the *IM* design namely the high thermal budget. Device structures that do not have any junctions in the *S*–channel–*D* path will hence be of interest for low cost optoelectronic applications. Several experimental studies have confirmed the low fabrication cost of the *JL* structure in comparison with the conventional *IM*

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designs [14–16]. To the best of our knowledge, no design approaches based on *JL* architecture and device global optimization were reported to achieve the high sensitivity and low power consumption. Hence, analytical drain current model is crucial not only in compact modeling but also for the modeling of the device *FoMs*, which is an essential topic for the comprehension of the device light controllability behavior. Furthermore, the device *FoMs* analytical models can be explored as a support to formulate the fitness functions for the global optimization considering both high sensitivity and low power consumption. After bringing evidence that the device analytical investigation is in fact needed, in this paper, a new *JL-OCFET* design is proposed as a new way to achieve both ultrasensitive and low power characteristics. To analyze the proposed device performance, accurate analytical models describing the device optical and electrical behavior are developed. The results showed that the analytical models are in good agreement with the 2-*D* numerical simulation over a wide range of device parameters [19]. Moreover, an overall performance comparison between both conventional *IM* and the proposed *JL* devices is carried out. Further, new insight based on global optimization is proposed to improve the device performance regarding both ultrasensitive and low power consumption aspects. The obtained results indicate the important role of the *JL* architecture for overcoming the trade-off between the high sensitivity and power consumption. This makes it a potential alternative for future low power and low cost optical photodetectors compatible with *CMOS* technology.

2. Modeling methodology

The junctionless design relies principally on the fact that the silicon channel and the source/drain regions are uniformly and highly doped regions, which are indicated by *n*+/*n*+/*n*+. Fig. 1 describes schematically the investigated *JL-OCFET* design, where the germanium gate is deposited on the *oxide*/*n-Si* structure. In order to acquire an initial band bending between the photosensitive gate and the silicon body, we consider the *Ge* gate with *p*-type doping concentration illuminated at normal incidence with a monochromatic light at the wavelength value of λ = 1.55 μm. For our analytical modeling, t_{Ge} and t_{Si} are the photosensitive *Ge* layer and the silicon thicknesses, respectively. *L* represents the channel length; N_d and N_a revel to the doping of the silicon channel and the *Ge* gate, respectively. In our analytical modeling procedure, the investigated *JL-OCFET* design is assumed as a long channel device, which allows us to reduce the Poisson's equation to a 1-*D* problem. Likewise, for achieving an excellent light controllability of the phototransistor channel conductivity, the silicon body is considered in our analytical modeling very thin (<40 nm). In the other side to avoid the quantum confinement effects the minimum channel thickness value is restricted by a limiting value equals to 10 nm (larger than 5 nm). Hence the silicon body is taken as (10 nm < t_{Si} < 40 nm). It is important to note that for the fabrication viewpoint, the proposed *JL* design involves a simple manufacturing process, where a simple epitaxial growth of the *Ge* on the *oxide*/n^+-*Si* structure is sufficient to develop the *JL-OCFET* design.

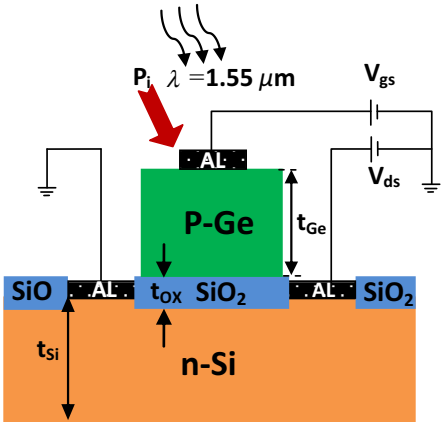

Fig. 1. Cross-sectional view of the proposed *JL-OCFET* phototransistor.

2.1. Drain current model

Poisson equation for an *N*-type device, with donor doping impurities is given by

$$\frac{d^2\Phi}{dx^2} = \frac{qN_d}{\varepsilon_{si}}\left(\exp\left(\frac{\Phi(x)-V}{V_t}\right)-1\right) \tag{1}$$

where q represents the electron charge, $\Phi(x)$ is the electrostatic potential, V_t is the thermal voltage which is equal to $\frac{KT}{q}$, V reveals to the potential shift across the silicon body, from source V_S (0) = 0 V to drain $V_D(L)$ and ε_{si} represents the silicon permittivity.

Under the condition of zero electric field at the end of the semiconductor film ($x = t_{si}$) that describes the fully depletion mode, the boundary conditions for determining the potential $\Phi(x)$ in our investigated structure can be given by

$$\Phi(0) = \Phi_s \tag{2-a}$$

$$\left.\frac{d\Phi}{dx}\right|_{x=t_{si}} = 0 \tag{2-b}$$

$$V(0) = 0 \tag{2-c}$$

$$V(L) = V_{ds} \tag{2-d}$$

where Φ_s reveals the surface potential, V_{ds} is the applied drain-source voltage.

By integrating Eq. (1) from $x = 0$ to $x = t_{si}$ and using the appropriate boundary conditions we can find the following equation

$$\left[\frac{d\Phi}{dx}\right]^2 = \frac{qN_dV_t}{\varepsilon_{si}}\left(\exp\left(\frac{\Phi_s-V}{V_t}\right)-\exp\left(\frac{\Phi_0-V}{V_t}\right)-\frac{\Phi_s-\Phi_0}{V_t}\right) \tag{3}$$

where Φ_0 represents the potential at $x = t_{si}$ and Φ_s is the surface potential.

Obviously, the gate voltage V_{gs} is divided between the insulator and the *Si* film; hence using the continuity of the electric flux at the *Oxide*/*n-Si* interface, we can find the surface potential as follows

$$\Phi_s = V_{gs}^* - V_{FB} - \frac{Q_m - Q_{fix}}{C_{ox}} \tag{4}$$

where Q_m and Q_{fix} refer to the mobile and the fixed charges respectively, the fixed charge can be estimated from $Q_{fix} = qN_dt_{si}$. The oxide capacitance C_{ox} can be calculated from $C_{ox} = \varepsilon_{ox}/t_{ox}$, with ε_{ox} and t_{ox} are the oxide permittivity and the oxide thickness, respectively. V_{FB} represents the flat band voltage which is principally related to both *Ge* and *Si* workfunctions and can be given as [9,10]

$$V_{FB} = \varphi_{Ge} - \varphi_{Si} + V_t \ln\left(\frac{N_d}{n_i}\right) \tag{5}$$

where φ_{Ge} and φ_{Si} are *Ge* and *Si* workfunctions, respectively, V_{gs}^* represents the optically modified gate voltage which is in our case mainly depending on the optically induced voltage V_{ph} and can be calculated from $V_{gs}^* = V_{gs} + V_{ph}$.

In order to estimate analytically the optically controlled voltage, it is essential to understand the operation mechanism of the proposed design. In this framework, under illumination with an