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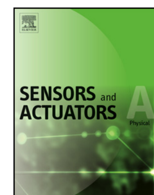

Effects of interface energy modification in solution-processed In_2O_3 thin film transistors for sensing applications☆

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ABSTRACT

Thin film transistors (TFTs) based on metal oxides have high mobility, transparency, and excellent stability, and are considered to be a key part of the next generation transparent electronic devices. Solution-processed metal oxide thin films using the sol-gel method has enabled the deposition of metal oxide thin films without a vacuum system, and it allows metal oxide TFTs to be fabricated more efficiently at low cost and over a large area through a simple process. In this study, we fabricated In_2O_3 using the sol-gel method and adopted various self-assembled monolayers (SAMs) to modify the interface between the semiconductor and dielectric layer. We used octadecyltrichlorosilane as a hydrophobic surface and partially removed it through exposure to UV radiation to form a patterned semiconductor using a simple spin-coating procedure that remarkably reduced the leakage current. 3-aminopropylsilane, (3-mercaptopropyl)trimethoxysilane, and cyclopentadienyltrimethylsilane as SAM materials and toluene and water as solvents to dilute them were used to modify the surface of the SiO_2. We measured the contact angle under various conditions and the electrical characteristics of the TFTs annealed in various temperatures of 230, 250, and 300 °C to confirm the effect of interface energy modification, and concluded that surface energy affected the mobility of the In_2O_3 transistors and the lower surface energy enhanced the mobility of the TFTs.

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1. Introduction

Over the last decade, oxide semiconductors have been extensively studied due to their good properties such as transparency, high mobility, and stability [1–8]. In addition, metal oxide semiconducting thin films can be deposited using the sol-gel method, which because of low cost is one of the benefits of using metal oxide semiconductors, and large-area deposition can be achieved by the solution process without using a vacuum system [9–12]. Furthermore, the sol-gel method is suitable for roll-to-roll processing, and it is possible to carry out simple and fast manufacturing of devices. Moreover, many researchers have demonstrated the application of oxide thin film transistors (TFTs) in sensors to detect pH [13], radiation [14], hydrogen [15], NO_2 [16], glucose [17], O_2 [18,19], H_2O [20], and ammonia and acetone [21]. While solution-processed metal oxide semiconductors have advantages, there is a challenge in terms of a low enough annealing temperature for flexible electronics [22]. To overcome this issue, Y. Kim et al. [23] attempted to decrease the annealing temperature by adopting photo-annealing instead of thermal annealing, while S. Jeong et al. [24] achieved a lower processing temperature by gallium doping of the indium zinc oxide.

In this study, we focused on surface energy modification, which is another aspect of the solution process with metal oxides. It is well known that the interface between the semiconducting and dielectric layers is a critical factor to determine the electrical characteristics of TFTs [25]. One of the most simple and effective methods to alter the interface properties is to form self-assembled monolayers (SAMs) with appropriate anchors and functional groups. We fabricated oxide TFTs using In_2O_3 and improved electrical properties by applying various SAMs between the SiO_2 surface and the In_2O_3 dielectric layer. Creating locally-varied surface energy facilitated patterning of the semiconducting layer through spin-coating, which in turn reduced the gate leakage current level of the TFTs. The different amounts of surface energy generated by the different functional groups of the SAMs and different solvents at the channel interface showed variation in the performance of the TFTs in various temperatures of 230, 250, and 300 °C. Furthermore, we analyzed the interface properties in correlation with the TFT performance.

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2. Experimental

A heavily doped Si wafer with thermally oxidized 100 nm-thick SiO_2 was used as a back gate and substrate, and was cleaned with acetone, ethanol, 2-popanol, and deionized water, each for 10 min in an ultrasonic bath to remove residue before deposition of the metal oxide layer. After cleaning, we carried out UV-ozone treatment for 30 min for further cleaning and improvement of adhesion between the substrate and the In_2O_3 precursor solution. Various surface treatments were carried out using silane materials with different functional groups: (3-aminopropyl)triethoxysilane (APTES), (3-mercaptopropyl)trimethoxysilane (MPTMS), and 3-chloropropyltriethoxysilane (CPTMS). The SAMs were diluted with toluene or deionized water, and the SiO_2 substrates were immersed in the solution. After this, the contact angle of water droplets on the SAM-treated substrates were checked to obtain information about the degree of hydrophobicity (Phoenix 300, Surface Electro Optics). After SAM treatment, we spin-coated the In_2O_3 precursor solution. For patterning of the In_2O_3 active layer, we used octadecyltrichlorosilane (OTS), which formed a hydrophobic surface on the SiO_2. Next, the OTS layer was eliminated using UV-ozone treatment for 30 min with a patterned shadow mask, which resulted in locally modified surface energy.

In order to synthesize metal oxide sol-gel, the indium(III) nitrate hydrate [$In(NO_3)_3 \cdot H_2O$] precursor was dissolved in 2-methoxyethanol to a concentration of 0.1 M. To form the In_2O_3 thin film on the substrate, we used spin-coating at 500 rpm for 5 s and at 3500 rpm for 35 s, and then residual solvent in the coated thin film was eliminated through annealing on a hotplate for 1 h in an air atmosphere. To investigate the effect of temperature on annealing, 230, 250, and 300 °C were selected as these are range of suitable annealing temperature for applications of flexible electronics compatible with plastic substrates [26]. 100 nm-thick Al electrodes as source and drain were deposited by thermal evaporation with a shadow mask.

The electrical characteristics of the In_2O_3 TFTs were measured using Agilent 4155C and reduced gate leakage was observed after patterning of the active layer.

3. Results and discussion

Fig. 1 shows the fabrication procedure of the In_2O_3 TFTs on an Si substrate with 100 nm-thick thermally oxidized SiO_2. To form OTS SAMs, the UV-ozone-treated substrate was dipped in OTS solution diluted in toluene, which changed the surface property of the SiO_2 to hydrophobic. A patterned active layer was formed by selective UV-ozone treatment, which was achieved using a shadow mask on the substrate. As a result, the UV-ozone-treated region showed hydrophilic properties whereas the region blocked from UV-ozone exposure remained hydrophobic properties. The indium(III) nitrate hydrate [$In(NO_3)_3 \cdot H_2O$] precursor was spin-coated only onto the hydrophilic surface due to the locally modified surface energy on the substrate. After spin-coating, samples were put onto a hotplate in air to form the In_2O_3 thin film and to eliminate residual solvent at either 230, 250, or 300 °C. The minimum temperature to form metal-oxygen bond from The indium(III) nitrate hydrate [$In(NO_3)_3 \cdot H_2O$] precursor by thermal annealing is 230 °C [27,28]. Although higher field effect mobilities would be achievable at higher annealing temperature [29] maximum process temperature is limited to 300 °C for plastic substrates to be applied for flexible electronics [30]. In order to confirm the effect of the In_2O_3 active layer patterning, we compared two fabricated In_2O_3 transistors by measuring their transfer curves.

Fig. 2a shows schematic pictures of the fully covered In_2O_3 active layer (above) and the patterned In_2O_3 active layer (below). For these transistors, the In_2O_3 active layers were annealed at 300 °C and the drain voltage was fixed at 30 V. Patterning of active layer is important for better performance in transistors since it prevents cross-talk between neighboring device elements and reduces parasitic resistance, which lead to low gate leakage current. Generally, wet-etching have been widely used to pattern oxide semiconductor layers. However, chemical etchant for wet-etching can damage the active layer to lower the performance and additional photolithography process is required, which result in increase of process cost. As shown in Fig. 2b, the transfer curves of the two devices concerning drain current corresponded regardless of patterning. However, the gate leakage current showed noticeably reduced values by patterning the In_2O_3 active layer since parasitic resistance through the fully covered semiconducting layer was reduced. We patterned active layer by orthogonality between hydrophilic and hydrophobic surface, which exclude use of chemical etchant and photolithography to remove the risk of damage by them. By using this patterning method with surface energy modification, process step and cost can be decreased. In addition, patterned active layer leads to improve the reliability and reproducibility of fabricated devices. The gate leakage current was reduced from 10^{-5} to 10^{-9} A, which is about 4 orders of magnitude, and showed a constant value along the gate bias (a similar value to the off current).

For the interface modification of the active layer area, various SAMs with different functionalities were employed (the molecular structures of the APTES, MPTMS, and CPTMS SAMs for the active layer interface are depicted in Fig. 3). After SAMs treatment, we observed changed surface properties on the SiO_2 substrate, which

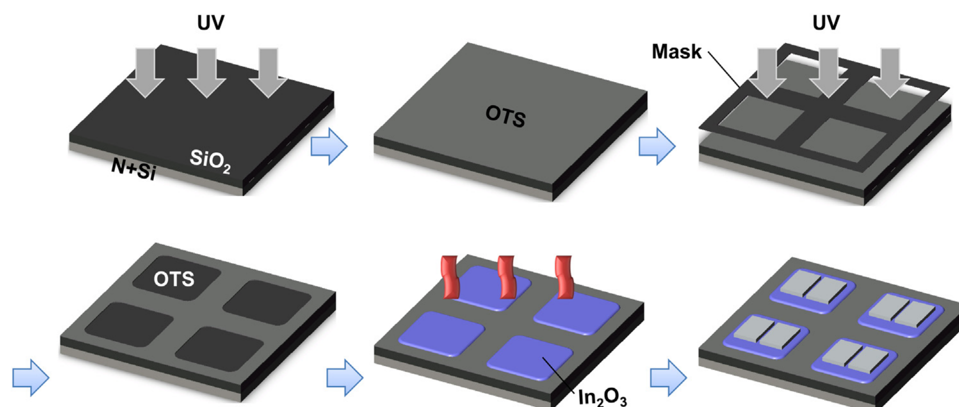

Fig. 1. Fabrication procedure of an In_2O_3 thin film transistor with a patterned substrate using OTS and UV treatment. 100 nm-thick Al used as source and drain was deposited by thermal evaporation. The channel length was 100 μm or 200 μm, and the channel width was 2000 μm.

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