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Accurate diode behavioral model with reverse recovery

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ABSTRACT

This paper deals with the comprehensive behavioral model of p-n junction diode containing reverse recovery effect, applicable to all standard SPICE simulators supporting Verilog-A language. The model has been successfully used in several production designs, which require its full complexity, robustness and set of tuning parameters comparable with standard compact SPICE diode model. The model is like standard compact model scalable with area and temperature and can be used as a stand-alone diode or as a part of more complex device macro-model, e.g. LDMOS, JFET, bipolar transistor. The paper briefly presents the state of the art followed by the chapter describing the model development and achieved solutions. During precise model verification some of them were found non-robust or poorly converging and replaced by more robust solutions, demonstrated in the paper. The measurement results of different technologies and different devices compared with a simulation using the new behavioral model are presented as the model validation. The comparison of model validation in time and frequency domains demonstrates that the implemented reverse recovery effect with correctly extracted parameters improves the model simulation results not only in switching from ON to OFF state, which is often published, but also its impedance/admittance frequency dependency in GHz range. Finally the model parameter extraction and the comparison with SPICE compact models containing reverse recovery effect is presented.

1. Introduction

The requirements on the accuracy of SPICE models are being continuously increased due to new branches, e.g. deep sub-micron technologies, high power applications, RF applications, etc. The main effort of model developers is of course focused on the development of MOSFET model. However, most of components including MOSFET contain one or more p-n junctions, which need to be precisely modeled, too. The new technologies and new applications with the accent on the high speed and low power consumption require SPICE device models to be accurate in full operating range, including high speed in combination with high voltage. One of the very important effects is the reverse recovery of p-n junction, where both the reverse current and the reverse voltage can be simultaneously large, which significantly affects the resulting power consumption. Unfortunately, standard compact SPICE models often neglect this effect, which can be crucial for some applications.

Fundamental reverse recovery modeling researches used in this paper have been published in [1–3]. Some of the recently published papers are focused to ultrafast diodes of various types, e.g., Si fast recovery diode, SiC Schottky barrier diode [4], or PIN diodes [5,6]. There also exist several studies focused to measurement methods of the reverse recovery time [7,8]. The reverse recovery is not naturally the domain of diode components only, but it also influences parasitic p-n junctions (parasitic diodes) of other components, where the most important category is the reverse recovery in high frequency power transistors, typically laterally diffused MOSFETs (LDMOS) [8–10]. The DC/DC converter can be considered one of typical applications, where the reverse recovery must be correctly modeled [11,12].

Some of resulting solutions however did not pass the convergence tests, results in some cases were not enough accurate or the solution contains reverse recovery effect only and does not cover other important phenomena, required for p-n junction modeling in production designs.

This paper demonstrates comprehensive behavioral model of p-n junction directly applicable to all common SPICE simulators supporting Verilog-A [13,14]. It deals with the basic equations, used solutions and test methods for the parameter extraction in time and frequency domains.

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2. Model development

2.1. Basic equations of compact SPICE diode model

This section deals with the set of well known basic diode equations, used as a ground for the behavioral model development. The goal of this section is not to describe full set of compact diode SPICE model equations and parameters, which can be found in each SPICE manual.

The total diode current in standard SPICE compact diode model is described as [15,16]

$$i = I_{\mathrm{pn}} + \frac{dQ_{\mathrm{inj}}}{dt} + \frac{dQ_{\mathrm{j}}}{dt} \tag{1}$$

where I_{pn} is the large signal current defined for $V > 0\mathrm{V}$ as [15,16]

$$I_{\mathrm{pn}}(V) = I_S\left(\exp\left(\frac{V}{nV_t}\right) - 1\right) \tag{2}$$

and for $V < 0\mathrm{V}$ as [15,16]

$$I_{\mathrm{pn}}(V) = I_S \tag{3}$$

where I_S is saturation current, n is emission coefficient and V_t is thermal voltage. Except the thermal voltage all these parameters are used as tunable compact SPICE model parameters.

Q_{inj} in (1) is charge of injected carriers, dominant mainly with positive voltage applied to p-n junction ($V > 0\mathrm{V}$), defined as [15,16]

$$Q_{\mathrm{inj}}(V) = T_T I_{\mathrm{pn}}(V) \tag{4}$$

where T_T is transit time used as a tunable compact SPICE model parameter. Derivative of this charge with respect to applied voltage is often denoted as the injection capacitance

$$C_{\mathrm{inj}}(V) = \frac{dQ_{\mathrm{inj}}}{dV} \tag{5}$$

Q_{j} in (1) is fixed charge of ionized dopant atoms, dominant mainly with negative voltage applied to p-n junction. This charge is stored in voltage dependent barrier or drift capacitance [15–17]

$$C_{\mathrm{j}}(V) = \frac{dQ_{\mathrm{j}}}{dV} = \frac{\mathrm{C_{J0}}}{\left(1 - \frac{V}{\mathrm{V_J}}\right)^{\mathrm{M_J}}} \tag{6}$$

where $\mathrm{C_{J0}}$ is the zero-bias junction capacitance, $\mathrm{V_J}$ is junction potential and $\mathrm{M_J}$ is a grading coefficient, all used as tunable compact SPICE model parameters.

In fact, (6) is actually not implemented in the SPICE programs. Instead of (6) a charge-controlled formulation of the junction capacitance is implemented, which can be obtained by an integration of $\mathrm{d}Q_{\mathrm{j}} = C_{\mathrm{j}}\mathrm{d}V$:

$$\int_0^{Q_{\mathrm{j}}} \mathrm{d}Q'_{\mathrm{j}} = \int_0^{V} \frac{C_{\mathrm{J0}}}{\left(1 - \frac{V'}{\mathrm{V_J}}\right)^{\mathrm{M_J}}} \mathrm{d}V'. \tag{7}$$

For evaluating this integral equation, let us make a substitution

$$1 - \frac{V'}{V_{\mathrm{J}}} = x \;\Rightarrow\; \mathrm{d}V' = -V_{\mathrm{J}}\mathrm{d}x, \tag{8}$$

which gives the integral

$$Q_{\mathrm{j}} = -V_{\mathrm{J}} \int_1^{1-\frac{V}{V_{\mathrm{J}}}} \frac{C_{\mathrm{J0}}}{x^m} \mathrm{d}x, v \tag{9}$$

to be solved, after that a final formula for the junction charge is obtained:

$$Q_{\mathrm{j}} = \frac{C_{\mathrm{J0}} V_{\mathrm{J}}}{1 - \mathrm{M_J}}\left[1 - \left(1 - \frac{V}{V_{\mathrm{J}}}\right)^{1-\mathrm{M_J}}\right]. \tag{10}$$

The formula (10) is actually implemented, and a current created by the junction capacitance is calculated in the standard way as $\dot{Q}_{\mathrm{j}}$.

Although the full set of diode model parameters contains a parameter called transit time, the T_T in (4) is not a real transit time. The transit time normally means an amount of time needed for carriers to travel at a finite velocity the distance from the middle of the diode to the external terminals. But SPICE model does not include such a concept, as it is clearly seen in (4). The stored injected charge Q_{inj} is an instantaneous function of the applied voltage.

2.2. Principle of reverse recovery behavioral model

Therefore, we were looking for a way to model the reverse recovery correctly. Several published lumped and behavioral models of reverse recovery were tested [1–3,10–12], but the simulation results of many of them were not satisfying. Either convergence or accuracy issues were observed during simulation. Finally the concept published in [1] was chosen.

The total diode current is there defined as

$$i = I_{\mathrm{inj}} + I_{\mathrm{j}} = \frac{dQ_{\mathrm{inj}}}{dt} + \frac{dQ_{\mathrm{j}}}{dt} \tag{11}$$

where I_{inj} is injection current defined as time derivative of the charge of injected carriers Q_{inj} and I_{j} is junction current defined as time derivative of the fixed charge of ionized dopant atoms Q_{j}.

Injection current I_{inj} is then in [1] expressed as

$$I_{\mathrm{inj}} = \frac{Q_{\mathrm{e}} - Q_{\mathrm{m}}}{T_{\mathrm{M}}} \tag{12}$$

where T_{M} is diffusion transit time used as a tunable model parameter, Q_{e} is the charge of carriers injected to the p-n junction and Q_{m} is the charge of carriers injected away from the p-n junction. Charges Q_{e} and Q_{m} are modeled by following equations [1]

$$Q_{\mathrm{e}} = \tau I_S \exp\left(\frac{V}{nV_t} - 1\right) \tag{13}$$

$$Q_{\mathrm{m}} = \tau I_{\mathrm{inj}} - \frac{d(\tau Q_{\mathrm{m}})}{dt} \tag{14}$$

where τ represening minority carrier lifetime is used as a tunable model parameter.

The injection capacitance from Eq. (5) can then be expressed as [1]

$$C_{\mathrm{inj}} = \frac{d(Q_{\mathrm{e}} - Q_{\mathrm{m}})}{dV} \tag{15}$$

The description of fixed charge of ionized dopant atoms Q_{j} as well as the drift capacitance C_{j} provided by (6) remain unchanged in the modified model.

2.3. Realization of model development

The reverse recovery model published in [1] has been developed in language MAST for Saber simulator, not compatible with SPICE simulators used, like ELDO, SPECTRE or HSPICE. So it was necessary to translate the model to more universal HDL language Verilog-A [13,14] applicable to most of standard SPICE simulators. However, the quite complex dependence between (12) and (14) demonstrated in Fig. 1 was found very difficult for the simulation and convergence in Verilog-A.

The first approach of dealing with this challenge was to use current controlled voltage source as a calculator for the charge Q_{m}. The charge Q_{m} from (12) became an auxiliary voltage to enable Verilog-A to

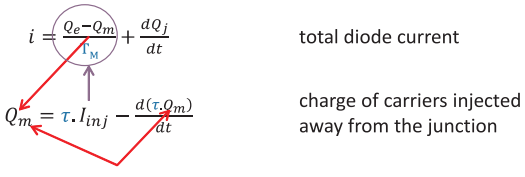

Fig. 1. Interdependencies in diode reverse recovery formulas.