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High-Performance and High-Reliability SOT-6 Packaged Diplexer Based on Advanced IPD Fabrication Techniques

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Abstract

A diplexer offering the advantages of compact size, high performance, and high reliability is proposed on the basis of advanced integrated passive device (IPD) fabrication techniques. The proposed diplexer is developed by combining a third-order low-pass filter (LPF) and a third-order high-pass filter (HPF), which are designed on the basis of the elliptic function prototype low-pass filter. Primary components, such as inductors and capacitors, are designed and fabricated with high Q-factor and appropriate values, and they are subsequently used to construct a compact diplexer having a chip area of 900 μm × 1100 μm (0.009 λ_0 × 0.011 λ_0, where λ_0 is the guided wavelength). In addition, a small-outline transistor (SOT-6) packaging method is adopted, and reliability tests (including temperature, humidity, vibration, and pressure) are conducted to guarantee long-term stability and commercial success. The packaged measurement results indicate excellent RF performance with insertion losses of 1.39 dB and 0.75 dB at operation bands of 0.9 GHz and 1.8 GHz, respectively. The return loss is lower than 10 dB from 0.5 GHz to 4.0 GHz, while the isolation is higher than 15 dB from 0.5 GHz to 3.0 GHz. Thus, it can be concluded that the proposed SOT-6 packaged diplexer is a promising candidate for GSM/CDMA applications. Synthetic solution of diplexer design, RF