



Endurance degradation and lifetime model of p-channel floating gate flash memory device with 2T structure



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ABSTRACT

The endurance degradation mechanisms of p-channel floating gate flash memory device with two-transistor (2T) structure are investigated in detail in this work. With the help of charge pumping (CP) measurements and Sentaurus TCAD simulations, the damages in the drain overlap region along the tunnel oxide interface caused by band-to-band (BTB) tunneling programming and the damages in the channel region resulted from Fowler-Nordheim (FN) tunneling erasure are verified respectively. Furthermore, the lifetime model of endurance characteristic is extracted, which can extrapolate the endurance degradation tendency and predict the lifetime of the device.

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1. Introduction

The floating gate flash devices are widely used as embedded nonvolatile memory in electronic equipment for low energy requests [1,2]. For the advantages of higher speed, better reliability and lower power consumption, the p-channel floating gate flash device is more competitive than the n-channel device, becoming one of the most popular commercial memory products [3–5]. Meanwhile, for the sake of eliminating the operating disturbance, two-transistor (2T) structure by adding a select gate (SG) is usually adopted [5–7]. In the past several decades, wide attentions have been paid on the reliability features including the endurance characteristic (that is programming and erasure cycling, P/E cycling) of floating gate flash device, and many studies have been reported on the electronic performances degradations related to the endurance procedure [8–12]. However, very few researches focus on the endurance degradation mechanisms of the specific p-channel floating gate flash device with band-to-band (BTB) tunneling programming and Fowler-Nordheim (FN) tunneling erasure, not to mention matching the tendency of the macroscopic electrical performance degradation with the microscopic tunnel oxide degradation during P/E cycling exactly. Moreover, the traditional cycling test standard for commercial memory product seems to take too much time

during wafer evaluation stage, and there are strong requirements for predicting the lifetime of the p-channel floating gate flash device and reducing the evaluation time [13].

In this work, the investigation on the endurance degradation mechanisms of the p-channel floating gate flash device with 2T structure is carried out by charge pumping (CP) measurements and Sentaurus TCAD simulations [14,15]. Furthermore, in order to predict the exact device endurance lifetime on wafer level, the lifetime model is extracted according to the endurance behaviors. It is recommended that by using the lifetime model, the endurance degradation amount of the device can be extrapolated, so that the evaluating time can get reduced.

2. Device structure and experiment

The device investigated in this work is manufactured by standard 180 nm flash process. The cross section is shown in Fig. 1. A 9 nm tunnel oxide is grown on an n-type substrate (Sub). An oxide-nitride-oxide (ONO) architecture is adopted as the dielectric to isolate the floating gate (FG) and the control gate (CG). A select gate (SG) is also deposited by the same process step with the CG to realize the function of select transistor. The effective channel length covered by the FG is 260 nm and the effective channel length of the select transistor is 300 nm, while the effective width of the device is 250 nm.

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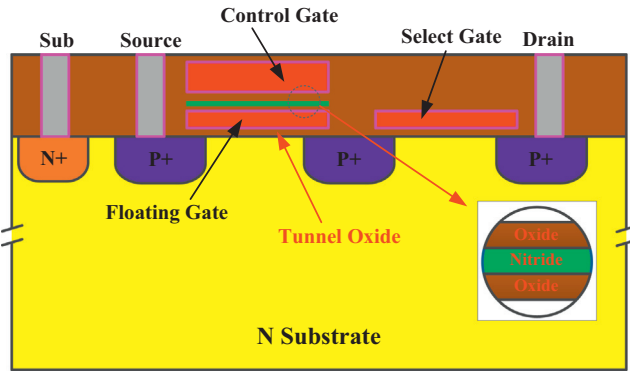


Fig. 1. Schematic cross section of the p-channel floating gate flash device with 2T structure.

The operating conditions of the flash device, including programming, erasure and threshold voltage (V_{th}) reading, are listed in Table 1. When the device is programmed, a pulse with -6.4 V amplitude and $1 \mu s$ width is applied to the drain, offering the required programming voltage along with an 8.8 V bias on the CG. Then the electrons will be injected into the FG by BTB tunneling mechanism. When it is needed to be erased, a -8.8 V pulse with 1 ms width is added to the CG, together with the 10.5 V substrate bias, swapping the electrons out of the FG by FN tunneling mechanism. The V_{th} is defined as the V_{cg} that induces the channel current to reach $0.1 \mu A$.

Fig. 2 shows the transfer characteristics of the flash device under programmed and erased states respectively. The programmed threshold voltage (V_{tp}) is more positive than the erased threshold voltage (V_{te}) for the FG storing electrons under programmed state. The V_{te} is negative because that the channel is p-type. The typical V_{tp} and V_{te} shown in Fig. 2 are 3.7 V and -4.3 V respectively.

An endurance test is conducted in this work to explore the degradation trend of the flash device. The programming and erasure conditions shown in Table 1 are added to the device in turn to realize P/E cycling. As the most concerned and critical parameters for the flash device, V_{tp} and V_{te} are measured under different time nodes to characterize the degradation up to 100k cycles.

3. Results and discussions

In this section, the endurance behaviors of both V_{tp} and V_{te} are presented. In order to explain this degradation trend and detect the damages caused by P/E cycling, the CP measurements are carried out at different cycling time nodes. Moreover, the simulations are performed to verify the degradation mechanisms extracted by CP measurements.

3.1. Degradation trends and descriptions

The endurance behaviors of V_{te} and V_{tp} after a 100 K cycling test are presented in Fig. 3. The V_{tp} exhibits an obvious negative shift while the V_{te} shifts to the positive direction slightly, and the P/E window ($V_{tp}-V_{te}$) gets closer along with the increase of cycling

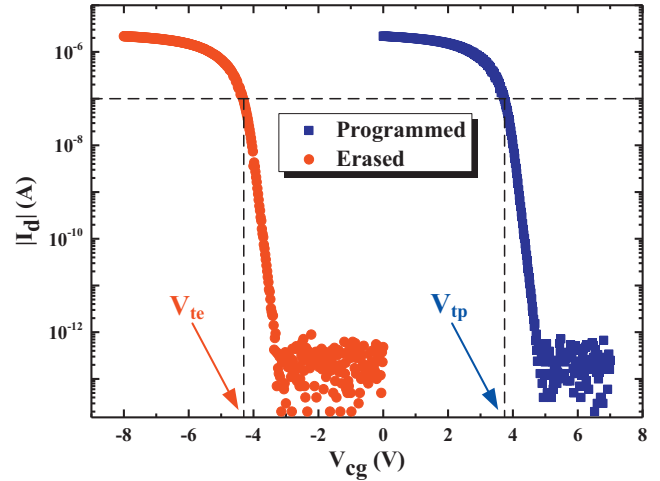


Fig. 2. Transfer characteristics of the flash device under programmed and erased states.

times. Moreover, the degradation degree of V_{tp} is more severe than that of V_{te} .

3.2. CP measurements and discussions

The CP measurements are usually employed to characterize the degradation along the Si/SiO₂ interface of gate-controlled devices, except for the p-channel floating gate flash device [15–19]. In this work, the CP method is adopted to detect the interface damages of the targeted p-channel floating gate flash device for the first time. However, due to the existence of the SG, the 2T-structure device has 5 terminals, and it cannot be measured by traditional 4-terminal CP method. It is because that when a constant voltage is applied to the SG, if the select transistor is off, the drain is floating and it cannot supply carriers. If the select transistor is on, the drain side of the memory transistor is not grounded due to the existence of coupling voltage from V_{sg} . Both of the situations will affect the accuracy of the CP results. Since the select transistor just plays a role as a switch in controlling the turn-on and turn-off of the storage transistor, it can be removed when analyzing the impacts of endurance stresses upon the tunnel oxide interface. Meanwhile, the stresses applied to the 1T-structure device and the 2T-structure device under operating conditions are almost same. Hence a 1T-structure floating gate device without the select transistor, which can be characterized by CP measurement, is manufactured by the same process in this work to help characterize the endurance degradations.

Fig. 4(a) shows the schematic diagram of CP measurement circuit with the 1T-structure p-channel floating gate flash device. The source and the drain are grounded while the CP signal is added to the CG. The CP current (I_{cp}) is measured from the substrate. Constant amplitude CP test condition is adopted [15]. The amplitude of the CP signal is 5 V while the base voltage (V_{base}) swaps from -9 V to 5 V, and the frequency is 5 MHz.

In order to get the appropriate CP measurement conditions, the gate voltages which induce $1 \times 10^{14} \text{ cm}^{-3}$ electrons (V_{ge}) and holes

Table 1
Operating conditions of the p-channel floating gate flash device with 2T structure.

	V_{sub} (V)	V_{cg} (V)	V_{sg} (V)	V_s (V)	V_d (V)
Programming	0	8.8	-8.4	-0.9	-6.4 (pulse width $1 \mu s$)
Erasure	10.5	-8.8 (pulse width 1 ms)	9.6	9.6	5
V_{th} reading (Programmed)	0	From 7 to 0	-3	0	-0.1
V_{th} reading (Erased)	0	From 0 to -8	-3	0	-0.1

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