



Submillimeter wave GaAs Schottky diode application based study and optimization for 0.1–1.5 THz



Sarvenaz Jenabi^{a,*}, Ali Malekabadi^a, Dominic Deslandes^b, Francois Boone^a, Serge A. Charlebois^a

^a Electrical Engineering Department, University of Sherbrooke, Sherbrooke, QC, Canada

^b Electrical Engineering Department, École de Technologie Supérieure, Montreal, QC, Canada

ARTICLE INFO

Article history:

Received 30 December 2016

Received in revised form 26 April 2017

Accepted 24 May 2017

Available online 31 May 2017

The review of this paper was arranged by Prof. S. Cristoloveanu

Keywords:

Schottky barrier diode

Submillimeter-wave devices

Terahertz

GaAs

Diode cut-off frequency

Parasitic capacitance

ABSTRACT

In this paper, a design and optimization method for submillimeter-wave Schottky diode is proposed. Parasitic capacitance is significantly reduced to under 20% of the total capacitance of the diode. The parasitic capacitance value is measured to be 0.6 fF for 1 μm anode radius which increased the cut-off frequency to 1.5 THz. A corresponding microfabrication process that provides higher degrees of freedom for the anode diameter, air-bridge dimensions and distance to the substrate is introduced and implemented. The DC and RF measurements are provided and compared with the simulations. In order to provide a better understanding of the diode behavior, the limiting factors of the cut-off frequency for different applications are studied and compared. For the mixer/multiplier mode, an improved and expanded formulation for calculation of the cut-off frequency is introduced. It is shown that the usable voltage bias range (with acceptable cut-off frequency) is limited by the exponential reduction of junction resistance, R_j , in mixer/multiplier mode.

© 2017 Elsevier Ltd. All rights reserved.

1. Introduction

There is great interest in the submillimeter-wave spectrum due to its numerous applications in astronomy, spectroscopy, security, surveillance, disease detection, DNA identification and telecommunication [1,2]. Lack of compact and efficient submillimeter-wave active and passive components slow down technological progress required for realization of the aforementioned applications. Neither design, simulation nor fabrication of these components are fully developed, with fabrication being the biggest challenge.

Diodes are critical elements in submillimeter-wave circuits. During recent decades, GaAs Schottky barrier diodes have been the preferred choice and have had the most significant progress. They are presently used in several submillimeter and terahertz (THz) circuits such as mixers [3–6], multipliers in solid state sources [6], phase shifters [7], and detectors [8]. For instance, in [6], an all solid-state monolithic multiplier chain of membrane diodes is presented where the multiplier chain employs four doubling steps to reach 1.5 THz from a 95 GHz input signal. This Schottky diode-based multiplier was developed to serve as a submillimeter-wave local oscillator for a heterodyne receiver.

Cut-off frequency is the main parameter in defining the behavior of a diode. It is estimated by $f_c = 1/2\pi C_j R_s$ where R_s and C_j are series resistance and junction capacitance respectively [10,11]. However, influence of other components of the diode equivalent circuit model and their bias dependency needs to be considered to achieve more accurate results. It is also of significant importance to provide an application-based study for the diode cut-off frequency since different sources of nonlinearity are targeted.

In order to expand the diode cut-off frequency to submillimeter-wave region, reducing the junction capacitance by shrinking the anode size has been the main approach [12–14]. However, aside from the junction capacitance, the parasitic elements such as parasitic capacitance, have high impact on the diode frequency performance and limit the cut-off frequency. For instance, in [15] the reported parasitic capacitance is 4–5 times larger than the junction capacitance. Therefore, the diode performance is mainly limited by its parasitic elements rather than the junction capacitance.

In this paper, four approaches for estimating the Schottky diode cut-off frequency for different applications are compared and discussed. In the third approach (mixer and multiplier applications) the cut-off frequency calculation method is improved and extended by considering all components of the diode equivalent circuit model and their respective bias dependencies. Moreover,

* Corresponding author.

E-mail address: jenabi.sarvenaz@gmail.com (S. Jenabi).

with the goal of minimizing the parasitic capacitance, a new design and optimization method is proposed. Furthermore, a novel micro-fabrication process which allows more flexibility and freedom in choosing the design parameters is introduced and implemented. The fabricated diodes are measured and compared to the simulations. The measurements results are in good agreement with simulations and confirm the benefits of the proposed optimization and fabrication methods.

2. Design and simulation

The design process starts by specifying the frequency range of operation. It is first necessary to define the electron mobility and plasma frequency. These parameters are used to select the appropriate semiconductor and its doping density. Then, based on wafer specifications, i.e., layers architecture and their properties including thickness, dopant and electron mobility, the performance of the diode can be simulated. A set of design parameters are assumed as the initial values and further optimizations are performed to achieve the desired characteristics. The input variables are semiconductor active layers (Schottky and n-well doped layers) doping, mobility, resistivity and their thicknesses, contact areas, shapes and their distance, both contact barrier heights, specific Ohmic-contact resistivity, operating frequency, and temperature.

The aforementioned calculations are accomplished by developing a code based on the analytical model of diode. The flowchart of the described design and optimization process is shown in Fig. 1. Fabrication limitations, such as achievable UV-lithography alignment and precision and having access to high mobility GaAs epitaxy wafers should be taken into account. Initial value of some parameters may be extracted from literature at the beginning to estimate and optimize requirements of epitaxy structure. After determining the epitaxy structure, the parameters (such as contacts barrier heights, specific contact resistivity, layers resistivity and mobility) are replaced by measurement results from quick tests such as TLM, C-V and Van-der-Pauw.

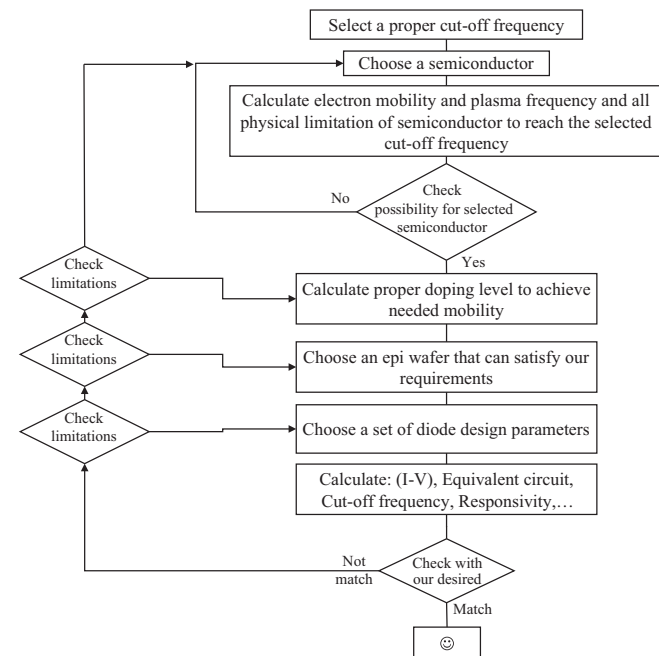


Fig. 1. Design and optimization process for Schottky diodes.

3. Optimization

The cut-off frequency of diodes and related operating frequency ranges are generally linked to the series resistance and junction capacitance through the $R_s \cdot C_j$ factor. Therefore, most of the literature focuses on decreasing the anode dimensions to reduce the junction capacitance, and thereby improve the cut-off frequency.

Fig. 2(a) shows the Schottky diode equivalent circuit. The diode parasitic components are identified for various parts of the device, as explained in Fig. 2(b). The total series resistance is $R_s = R_{sl}(V) + R_{sub} + R_{p1} + R_{p2}$ in which only R_{sl} has dependency to voltage bias. R_{sl} represents the part of the Schottky layer that is not depleted and therefore grows sub-linearly with the voltage bias across the junction. The junction capacitance C_j and the resistance R_j are the heart of the Schottky diode, which their voltage-dependency generates its nonlinear characteristic.

The total capacitance is defined as $C_T = C_j(V) + C_p = C_j(V) + C_{fp} + C_{foh} + C_{pp}$, where C_p is the sum of all parasitic capacitances. In this work, the impact of C_p on the cut-off frequency is taken into account by considering the total capacitance C_T instead of C_j . Although C_p and C_j , as shown in Fig. 2, are not exactly in parallel, C_T gives a good estimation of the diode total capacitance and practical cut-off frequency. By reducing the junction capacitance, C_T is dominated by parasitic term that becomes the main limitation of the device. In many cases the parasitic capacitance is shown to be several times larger than the junction C_j itself. For example, in

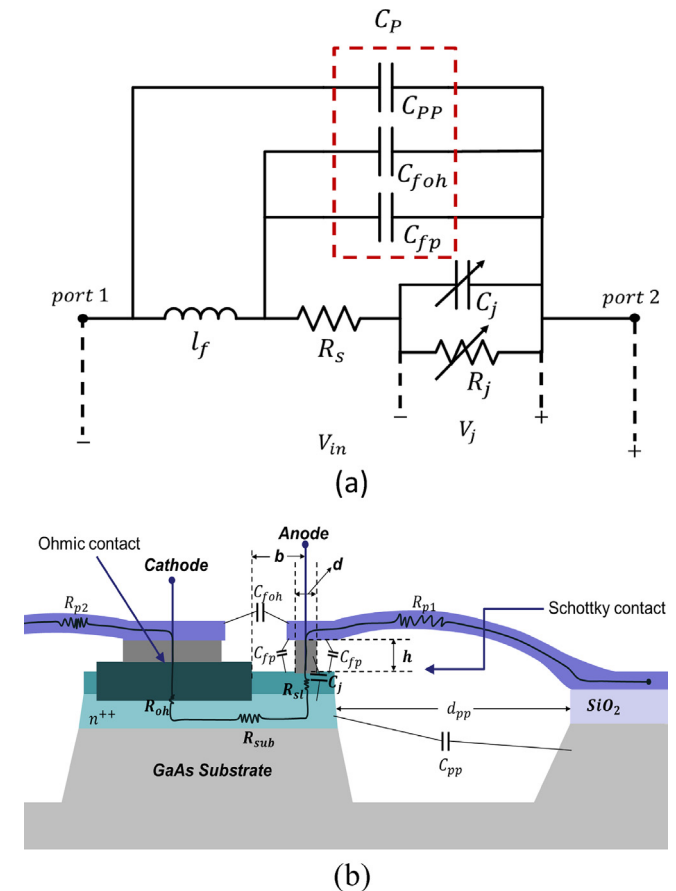


Fig. 2. (a) Diode equivalent circuit model. C_{pp} is the pad-to-pad parasitic capacitance, C_{fp} is the capacitance between finger and mesa, and C_{foh} is the capacitance between finger and the Ohmic contact; (b) schematic of diode side view and equivalent circuit components. Parasitics R_{p1} , R_{p2} , R_{oh} , R_{sub} and R_{sl} are anode finger, Ohmic air-bridge, Ohmic contact, n-well doped channel and the un-depleted Schottky layer resistance, respectively.

Download English Version:

<https://daneshyari.com/en/article/5010179>

Download Persian Version:

<https://daneshyari.com/article/5010179>

[Daneshyari.com](https://daneshyari.com)