Accepted Manuscript

Surface Potential based Modeling of Charge, Current, and Capacitances in DGTFET including Mobile Channel Charge and Ambipolar Behaviour

Prateek Jain, Chandan Yadav, Amit Agarwal, Yogesh Singh Chauhan

PII: S0038-1101(17)30081-3
DOI: http://dx.doi.org/10.1016/j.sse.2017.05.012
Reference: SSE 7237

To appear in: *Solid-State Electronics*

Received Date: 26 January 2017
Revised Date: 26 May 2017
Accepted Date: 30 May 2017

Please cite this article as: Jain, P., Yadav, C., Agarwal, A., Chauhan, Y.S., Surface Potential based Modeling of Charge, Current, and Capacitances in DGTFET including Mobile Channel Charge and Ambipolar Behaviour, *Solid-State Electronics* (2017), doi: http://dx.doi.org/10.1016/j.sse.2017.05.012

Surface Potential based Modeling of Charge, Current, and Capacitances in DGTFET including Mobile Channel Charge and Ambipolar Behaviour

Prateek Jain[a,*], Chandan Yadav[a], Amit Agarwal[b], Yogesh Singh Chauhan[a]

[a]Department of Electrical Engineering, Indian Institute of Technology Kanpur, Kanpur India-208016
[b]Department of Physics, Indian Institute of Technology Kanpur, Kanpur India-208016

Abstract

We present a surface potential based analytical model for double gate tunnel field effect transistor (DGTFET) for the current, terminal charges, and terminal capacitances. The model accounts for the effect of the mobile charge in the channel and captures the device physics in depletion as well as in the strong inversion regime. The narrowing of the tunnel barrier in the presence of mobile charges in the channel is incorporated via modeling of the inverse decay length, which is constant under channel depletion condition and bias dependent under inversion condition. To capture the ambipolar current behavior in the model, tunneling at the drain junction is also included. The proposed model is validated against TCAD simulation data and it shows close match with the simulation data.

Keywords: Band-to-Band Tunneling (BTBT), Tunnel Field Effect Transistor (TFET), Surface Potential, Terminal Capacitance.

1. Introduction

Tunnel field effect transistor (TFET) is considered to be a promising device to overcome the shortcoming of conventional MOSFET on account of its exceptional leakage power performance [1]. The growing interest of the device community in low power applications has lead to an extensive amount of experimental and simulation work on TFETs [2, 3, 4]. Currently, the major drawback of TFETs from an application point of view is i) low ON current (I_{ON}), ii) higher ambipolar current, and iii) complex fabrication steps compared to the conventional MOSFET. However, with time, different techniques have been reported to improve the TFET device characteristics [5, 6, 7, 8, 9, 10, 11]. To facilitate the use of TFETs in circuit design, an accurate analytical/compact model for TFET is needed, which is also computationally efficient. While there have been significant efforts to develop an analytical/compact model for TFETs, there is still considerable scope for improvement.

A good TFET model should capture the device electrostatics accurately, and predict the ambipolar drain current along with the terminal charges and capacitances accurately in both the depletion as well as inversion regime, while being computationally efficient for circuit simulations.

Earlier models based on 1-D Poisson equation do not accurately capture the electric field distribution in short channel devices [12]. Pseudo 2-D method based TFET models capture the electrostatics correctly, but some of them are valid either only for depletion conditions [13, 14, 15, 16, 17, 18], while some do not model the ambipolar current [13, 14, 15, 19] and some do not model the terminal charges and capacitances [15, 16, 17, 18, 19, 20]. Additionally, there are some empirical drain current and capacitance model for TFETs as well [21, 22, 23], however

*Corresponding author at: Indian Institute of Technology Kanpur, India
Email address: prateekj@iitk.ac.in (Prateek Jain)