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PLL application research of a broadband MEMS phase detector: Theory, measurement and modeling

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ABSTRACT

This paper evaluates the capability of a broadband MEMS phase detector in the application of phase locked loops (PLLs) through the aspect of theory, measurement and modeling. For the first time, it demonstrates how broadband property and optimized structure are realized through cascaded transmission lines and ANSYS simulations. The broadband MEMS phase detector shows potential in PLL application for its dc voltage output and large power handling ability which is important for munition applications. S-parameters of the power combiner in the MEMS phase detector are measured with S_{11} better than −15 dB and S_{23} better than −10 dB over the whole X-band. Compared to our previous works, developed phase detection measurements are performed and focused on signals at larger power levels up to 1 W. Cosine tendencies are revealed between the output voltage and the phase difference for both small and large signals. Simulation approach through equivalent circuit modeling is proposed to study the PLL application of the broadband MEMS phase detector. Synchronization and tracking properties are revealed.

1. Introduction

A phase-locked loop is a feedback system consisting of a phase detector, a loop filter and a voltage controlled oscillator [1,2]. It can accurately track the applied frequency- or phase-modulated signal, realize frequency tuning and generate a stable frequency output. Any system, including wireless base station, pager and local oscillator, that require a stable frequency can benefit from the PLL technique. A significant application example of PLL is a receiver [3,4] applied in radar or electronic countermeasures system. Fig. 1 gives an illustration of a typical receiver for satellite positioning. High performance receivers for such munition applications [5,6] generally have stringent requirements for wide bandwidth, large dynamic range and excellent power handling ability especially for large power signals, which are generally utilized to interfere and damage electronic devices.

According to the researches in the recent past, MEMS technique offers better performance and reliability in the aspects of power consumption, sensitivity to temperature, linearity and bandwidth [7]. There have been considerable interests in micro-electromechanical system (MEMS) based sensors and devices as feasible alternatives to traditional on-chip components for both civil and military use [8,9]. The viable of MEMS oscillators in the application of PLL have been investigated [10,11]. Existing technologies of phase detectors are based on diodes [12] and multipliers [13], which are both suffered from low cut-off frequency and non-linear distortion at large inputs. In comparison, single band MEMS phase detectors fabricated by our group show superiorities in PLL application [14–17], for they are generally featured with lower power consumption, higher operating frequency and ability to handle larger power levels. In order to meet the demands of broadband needs, MEMS phase detector for the whole X-band, 8–12 GHz, has also been presented by our group [18].

Therefore, this paper evaluates the capability of the broadband MEMS phase detector in the application of a PLL. As Ref. [18] only delivers a preliminary comprehension of the phase detection property with small input powers beyond 200 mW, this paper presents an integrated study related to its design theory, developed measurements for large signals and equivalent-circuit modeling of a PLL based on it. This broadband MEMS phase detector is constructed by a broadband power combiner and a terminating-type power sensor. In the power combiner, which is the key factor to determine the bandwidth, two sections of ACPSs are cascaded to realize broadband performance. Detailed design equations are deduced by even- and odd-mode analysis. The terminating-type power sensor, which determines the detection sensitivity, gets its optimized structure through simulations in ANSYS software.

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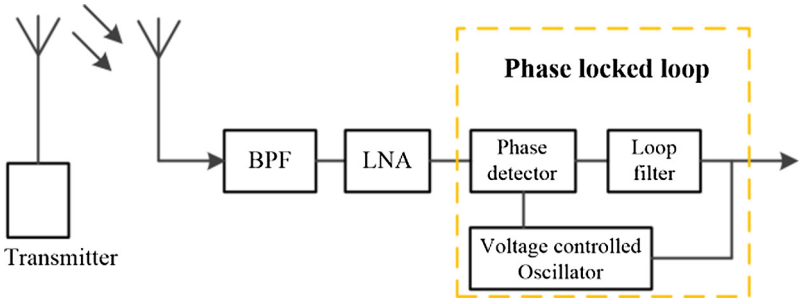

Fig. 1. A receiver system based on a phase locked loop for munition applications.

Measured S-parameters for the power combiner show −15 dB return loss and −10 dB isolation over X-band. Phase detection capabilities from small signals 10 mW up to large signals 1 W are measured. Cosine tendencies are both revealed. Frequency dependent measurements are conducted to verify the broadband performance. An equivalent circuit model of a PLL based on the broadband MEMS phase detector is proposed. Synchronization and tracking properties are revealed through simulation.

2. Theory and design

The schematic diagram of the broadband MEMS phase detector is depicted in Fig. 2. It composes a broadband power combiner and a terminating-type power sensor.

The power combiner inside the MEMS phase detector is composed of two symmetrical input ports (Port 2 and Port 3), one output port (Port 1) and transmission lines of cascaded two-sections of asymmetrical coplanar strips (ACPSs). It performs a vector combination [19] function to the input signals. The power P of the combined signal is determined by the amplitudes of the two input signals and the phase difference between them.

$$P = \frac{V_i^2 + V_o^2 + 2V_iV_o\cos\Delta\varphi}{2Z_0} \tag{1}$$

$$\Delta\varphi = (\omega_i - \omega_o)t + \varphi_i - \varphi_o \tag{2}$$

where V_i and V_o are the magnitudes of the two input signals, respectively, $\Delta\varphi$ symbolizes their phase difference.

The CPW at the output port of the power combiner feeds the combined signal to the terminating-type power sensor. The load resistors act as absorbing media to convert the energy into heat. As the heat transfers, temperature gradient will be established along the thermopile. The hot junctions of the thermopile are near, while the cold junctions are far away from, the load resistors. Temperature difference between the hot and cold junctions of the two different materials in the thermopile will result in a dc voltage V at the output pads, which is known as Seebeck effect [20].

$$V = (\alpha_1 - \alpha_2)\sum(T_h - T_c) = R_{th-e}\frac{V_i^2 + V_o^2 + 2V_iV_o\cos(\Delta\varphi)}{2Z_0} \tag{3}$$

where α_1 and α_2 are the Seebeck coefficient, T_h, T_c are the temperatures of the hot and cold junctions, $R_{th\text{-}e}$ is the equivalent total thermal resistance of the power sensor.

As no high-frequency element is included in the output of the MEMS phase detector, it shows the potential of acting directly as the control voltage of a VCO in the application of PLL. The output frequency ω_{ins} of the VCO can be expressed as

$$\omega_{ins} = K_vR_{th-e}\frac{V_i^2 + V_o^2 + 2V_iV_o\cos(\Delta\varphi)}{2Z_0} + \omega_o \tag{4}$$

where K_v is the gain factor of the VOC and ω_o is its center frequency. As can be deduced, the variation range of the VCO output frequency and the pull-in range of the PLL are determined by the output V of the MEMS phase detector and the gain factor kV of the VCO.

In order to be applied in a PLL successfully, reasonable design should be implemented to the broadband MEMS phase detector. A broadband power combiner can benefit the phase detector with stable detection property over a wide bandwidth. Meanwhile, optimized structure of the terminating-type power sensor can facilitate high detection sensitivity.

According to [21,22], a broadband power combiner can be obtained by substituting the quarter-wavelength line in traditional structure [23] with cascaded two- or multi-sections of transmission lines. In this paper, two sections of ACPSs are connected between the combine port (Port 1) and the symmetrical input ports (Port 2 and Port 3) as shown in Fig. 2. The ACPSs are characterized by impedances Z_1, Z_2 and lengths l_1, l_2, respectively. Isolation between Port 2 and Port 3 is achieved via two resistors R_1 and R_2. The values of Z_1, Z_2 and l_1, l_2 are supposed to be designed to yield optimum behaviors at f_1 and f_2, and obtain excellent response over the bandwidth between them. Analysis method of even- and odd-mode can be adopted to achieve the above demands.

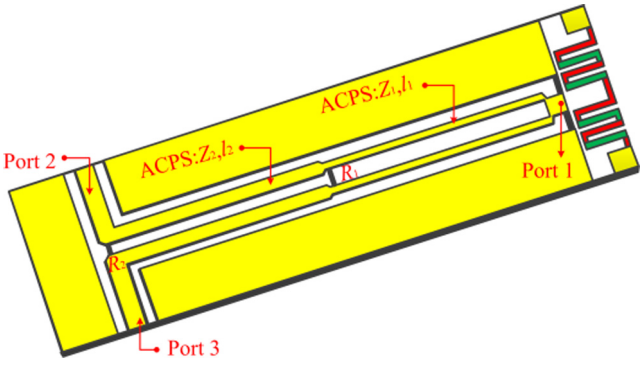

Fig. 2. Schematic diagram of the MEMS broadband phase detector.

In even-mode analysis, as represented by the bisected circuit depicted in Fig. 3(a), the input signals at Port 2 and Port 3 are characterized by equal magnitude and phase. Therefore, the resistors R_1 and R_2 are open circuited for no current flows through them. The input impedance Z_{in}^e at Port 1 is given by the following equations

$$Z_{in}^e = Z_1\frac{Z_L + jZ_1\tan(\theta_1)}{Z_1 + jZ_L\tan(\theta_1)} \tag{5}$$

$$Z_L = Z_2\frac{Z_0 + jZ_2\tan(\theta_2)}{Z_2 + jZ_0\tan(\theta_2)} \tag{6}$$

where θ_1 and θ_2 represent the corresponding electrical lengths of the ACPSs, respectively.