Solid-State Electronics 132 (2017) 24–30

Contents lists available at ScienceDirect

Solid-State Electronics

journal homepage: www.elsevier.com/locate/sse

3-D multilayer monolithic integration of vertical-oriented double-heterojunction GaAs based pHEMT and thermal influence on device parameters

Mohammad A. Alim [a,*], Ali A. Rezazadeh [b]

[a] Applied Physics, Electronic and Communication Engineering, University of Chittagong, Bangladesh
[b] Microwave and Communication Systems Research Group, The University of Manchester, M13 9PL, UK

ARTICLE INFO

Article history:
Received 3 January 2017
Received in revised form 28 February 2017
Accepted 1 March 2017
Available online 6 March 2017

The review of this paper was arranged by Prof. E. Calleja

Keywords:
AlGaAs/InGaAs/GaAs based pHEMTs
3-D MMICs
Multilayer fabrication
Characterisation
Thermal influence

ABSTRACT

This study focuses on 3-D multilayer monolithic integration of vertical-oriented double-heterojunction AlGaAs/InGaAs/GaAs based pseudomorphic high electron mobility transistors. The effects of the presence of 3-D components above the active layer were accomplished by comparing three multilayer fabricated device of different thickness with a virgin device where the thickness of the 3-D components e.g., both metal and polyimide layer were varied. The output current, on-state gate leakage, transconductance are found to be decrease with the increase in thickness of the 3-D components and on the other hand, the on-state resistance, knee voltage and off-state gate leakage is increased. Lastly, the thermal influences on the device behaviour such as off-state and on-state gate leakage, barrier inhomogeneities at Schottky contacts, zero temperature coefficients at the transfer curve, and the threshold voltage as a function of drain bias were measured and analyzed for the both pre and post fabricated multilayer devices. These effective comparisons in terms of thickness and temperature of the both device are useful for future designs and optimizations of multilayer vertical stacked 3-D MMICs.

1. Introduction

Three-dimensional multilayer vertical-stacked monolithic microwave integrated circuits (3-D MMICs) technique is an up-and-coming device technology to fulfil the demand of current semiconductor market such as low cost, high integration levels and high performance, simpler, and more rapid development [1]. A 3-D structure offers several other benefits, including compactness and the isolation of passive components from substrate properties using the ground plane. Owing to the disadvantages of the conventional CPW structures includes limited degree of size reduction, complex circuit designs, grounds must be on either side of the signal line, very high current density at the signal line edges resulting in high conductor losses [2]. The vertical-stacked 3-D MMICs technology is implemented to overcome this problem, which refers to structures that are deposited several metal layers are sandwiched by insulators in vertical order [3,4]. This is a chip for complicated circuits with large number of active components and passive components are built on a semi-insulating GaAs substrate. With multilayer technology, passive components are transformed from horizontal to vertical plane to create a miniaturised 3-D structure wafer [5] (see fig. 1). This way reduced the chip size and production cost without disturbing the devices performance. An adequate partition between the application circuit process and the semiconductor active device process are possible and hence lessen the turnabout time. Compact MMIC components were fabricated using a seven-layer fabrication procedure on semi-insulating GaAs substrate with pseudomorphic high electron mobility transistors (pHEMTs) being pre-fabricated on the top of it. The integration of active and passive components can be realised by opening the silicon nitride (Si_3N_4) windows of the pre-fabricated (virgin) pHEMTs so that sandwiched layers of metal and dielectric can be deposited to create multilayer MMICs [6]. Fig. 1 represents the design and fabrication of compact multilayer CPW components and circuits on semi-insulating GaAs substrate. 3-D MMICs are realised on a semi-insulating GaAs substrate by stacking two dielectric layers separated by three metal conductor layers. A number of passive components, such as thin film resistors, inductors, capacitors and CPW-to-TFMS transitions, were designed and realised.

* Corresponding author at: Applied Physics, Electronic and Communication Engineering, University of Chittagong, Bangladesh.
E-mail addresses: mohammadabdulalim@cu.ac.bd (M.A. Alim), ali.rezazadeh@manchester.ac.uk (A.A. Rezazadeh).

http://dx.doi.org/10.1016/j.sse.2017.03.001
0038-1101/

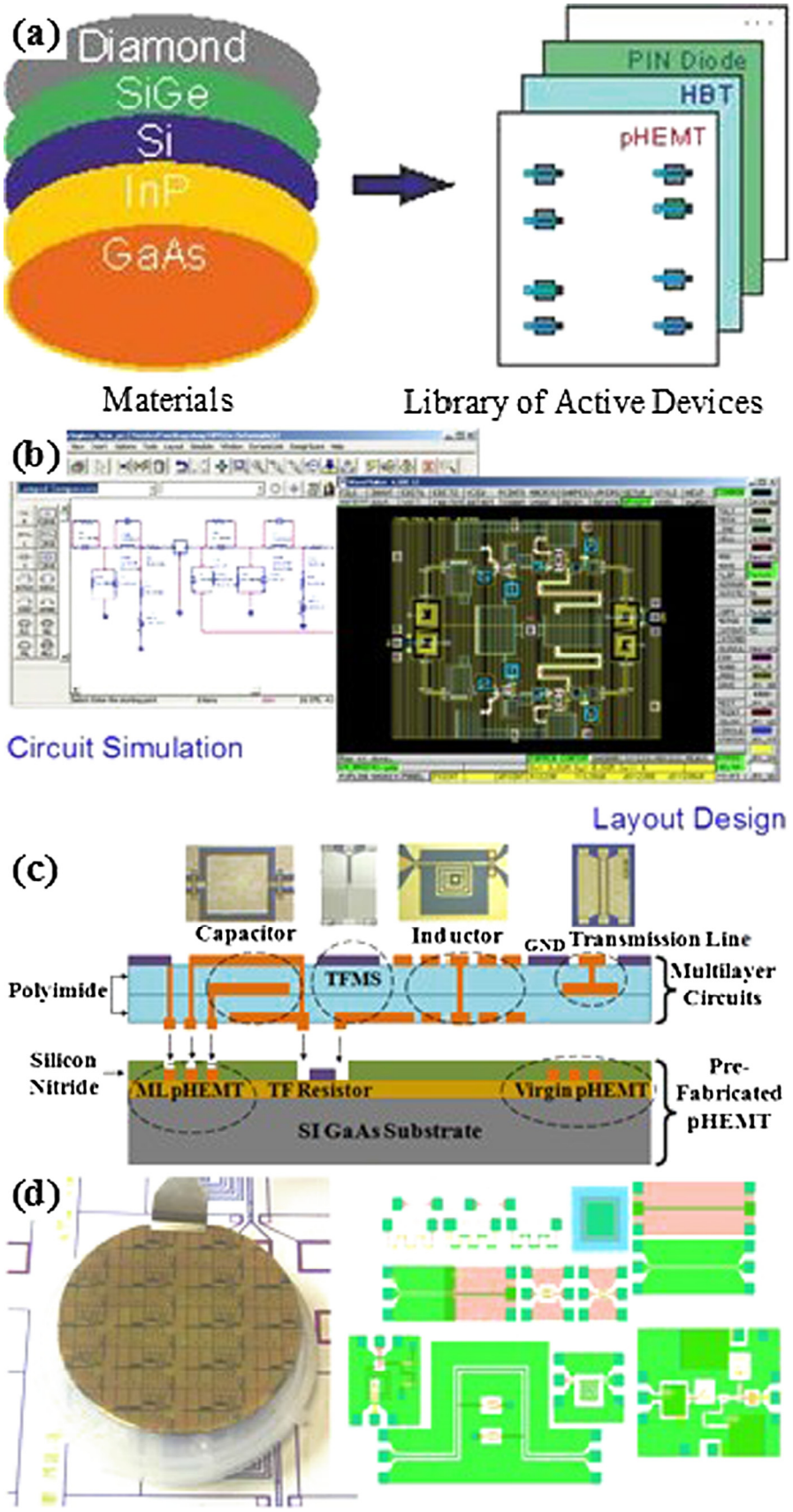

Fig. 1. 3-D multilayer MMICs design, fabrication and realization: (a) active components, (b) layout design and simulation, (c) horizontal to vertical transformation of the passive components, and (d) multilayer fabrication.