



Study on the influence of γ -ray total dose radiation effect on the electrical properties of the uniaxial strained Si nanometer NMOSFET



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ABSTRACT

The carrier microscopic transport process of uniaxial strained Si n-channel metal-oxide semiconductor field-effect transistor (NMOSFET) has been analyzed under γ -ray radiation. The variation of electrical characteristics of the uniaxial strained Si nanometer NMOSFET has also been investigated under the total dose radiation. The Capacitor-Voltage (C-V) and Current-Voltage (I-V) characteristics are measured at room temperature before and after irradiation for each sample. The results indicate that the drift of threshold voltage, the degradation of carrier mobility and the increase in leakage current because of the total dose radiation effect. Moreover, a two-dimensional analytical model of threshold voltage (V_{th}) and carrier mobility model have been developed due to the total dose irradiation taken into consideration. Based on the model, numerical simulation has been carried out by MATLAB. The influence of the total dose, geometry and physics parameters on threshold voltage was simulated. Moreover, to evaluate the validity of the model, the simulation results were compared with experimental data, and good agreements were confirmed. Thus, the experiment results and proposed model provide good reference for research on irradiation reliability and application of strained integrated circuit of uniaxial strained Si nanometer n-channel metal-oxide semiconductor field-effect transistor.

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1. Introduction

Strained technology has been widely used to improve the performance of Si CMOS devices, and strained-Si technologies have caught much attention as device size is scaling down [1–4]. Ionizing radiation can induce significant charge build-up in these oxides and insulators leading to device degradation and failure. In space systems (and other harsh radiation environments, e.g., high-energy particle accelerators), exposure to high fluxes of electrons and protons can significantly reduce system lifetime due to total ionizing dose. Over the last thirty years, the effects of total ionizing dose on radiation-induced charge build-up in oxides have been investigated in detail [5]. Hence, researches on the irradiated electrical characteristics and the radiation hardening technique of the strained Si MOSFET device are of great significance [6–9]. A number of studies have reported the influence of radiation on electrical properties of strained Si MOSFET [10–13], which were based on experiment but lack of mature theory. The shift of the threshold voltage (V_{th}) and the increased leakage current level are research hotspots for irradiated strained Si MOSFET device. V_{th} and carrier mobility are important electrical parameters of a device, and have

been studied extensively. One-dimensional model on V_{th} of the biaxial strained Si has been reported before [14]. As devices continue to downscale, their performance cannot be characterized by one-dimensional model of V_{th} . Therefore, a two-dimensional (2D) model needs to be further considered. However, the 2-D model on V_{th} of the uniaxial strained Si nanometer NMOSFET has rarely been reported.

Capacitor-voltage and current-voltage properties are measured at room temperature in this paper, aiming to compare the oxide trapped charge, interface trapped charge density and leakage current before and after gamma-ray irradiation. Moreover, we propose a two-dimensional analytical model on V_{th} and carrier mobility model of the uniaxial strained Si nanometer NMOSFET due to the total dose radiation. The results from the model are compared with the experimental data and they are found to be in good agreement. Thus, the model can provide valuable reference for research on irradiation reliability and application of strained integrated circuit of uniaxial strained Si nanometer n-channel metal-oxide semiconductor field-effect transistor.

2. Experiment

The devices considered in this study are MOS structure with TiAl gate contact, High-K dielectrics, and p-type silicon substrates.

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Relaxed Si nanometer NMOSFET and uniaxial strained Si nanometer NMOSFET devices were fabricated, the difference being the uniaxial strained Si nanometer NMOSFET device using a cap layer of thin silicon nitride film. The micrograph of the uniaxial strained Si nanometer NMOSFET device is shown in Fig. 1. Due to the large lattice mismatch between Si and HfO₂, a thin layer of silicon oxide of natural oxidation is grown before the growth of HfO₂, and the growth of HfO₂ is used in atomic layer deposition method. The real thicknesses of the SiO₂ and HfO₂ are close to 0.3 nm and 4.4 nm, respectively. In order to restrain the two level physical effects caused by small size device, the device structure is carried out by LDD and HALO injection. The scale dimension and material parameters of the device are as follows: the oxide layer is SiO₂ and HfO₂, the equivalent oxide thickness being 1 nm. The junction depth of source/drain region, the gate length and gate width are 25 nm, 50 nm and 3 μ m, respectively. Fig. 2 shows schematic cross section of uniaxial strained Si nanometer NMOSFET indicating the build-up of radiation-induced oxide trapped charge and the generation of interface traps.

The device of uniaxial strained Si nanometer NMOSFET is irradiated using a ⁶⁰Co γ -ray laboratory source at a constant dose rate of 0.5 Gy (Si)/s. The TID is deposited in several steps up to a maximum of 2.5 KGy. Electrical measurements are performed at each TID step. All irradiated samples are measured using field test, and are required to finish measurement within 30 min, in order

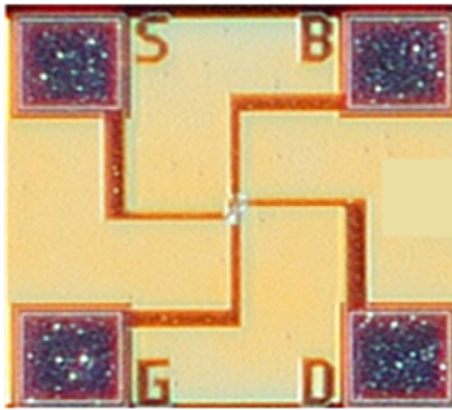


Fig. 1. Micrograph of uniaxial strained Si nanometer NMOSFET device.

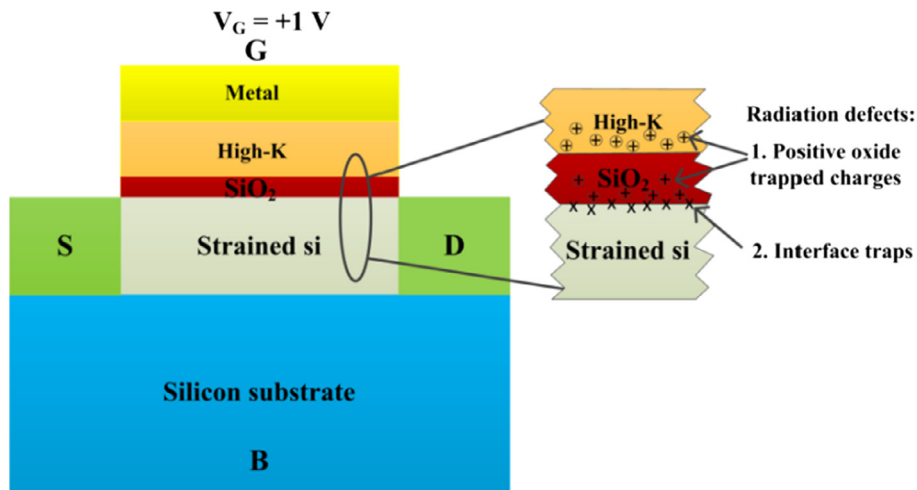


Fig. 2. Schematic cross section of uniaxial strained Si nanometer NMOSFET indicating the build-up of radiation-induced oxide trapped charge and the generation of interface traps.

Table 1

The V_t shift of relaxation and uniaxial strain Si nanometer NMOSFET device under the absorbed dose.

Dose/KGy	0.5	1.0	1.5	2.0	2.5
$\Delta V_{th,si}/V$	-0.0352	-0.0403	-0.0410	-0.0415	-0.0431
$\Delta V_{th,ssi}/V$	-0.0354	-0.0405	-0.0408	-0.0417	-0.0428

to reduce the annealing effect and ensure the accuracy of the test data. Static drain-current I_D vs gate-voltage V_{GS} electrical characteristics are measured with a HP4155B parametric analyzer. Some parameter extractions presented come from these static measurements including the threshold voltage V_{th} , the trans-conductance g_m and the leakage current I_{OFF} (I_D at $V_{GS} = 0$ V and $V_{DS} = V_{DD}$). Irradiation bias: $V_G = +1$ V, drain voltage V_D is equal to source voltage V_S ($V_D = V_S = 0$). Measurement bias: $V_G = 0-1$ V, scanning voltage $V_{step} = 0.05$ V, $V_D = 50$ mv, $V_S = 0$.

The V_{th} shifts of relaxed nanometer Si NMOSFET and uniaxial strained Si nanometer NMOSFET device with different absorbed doses are listed in Table 1. As can be seen in Table 1, the V_{th} drift of relaxed Si nanometer NMOSFET is similar to that of uniaxial strained Si nanometer NMOSFET. It can be inferred that the stress does not change after irradiation, and the experimental results are in good agreement with the previous reports [15].

3. Two-dimensional threshold voltage model and carrier mobility model

The schematic structure of uniaxial strained Si NMOSFET is shown in Fig. 3.

When the uniaxial strained Si NMOSFET is exposed to γ -ray, electron-hole pairs are created in the oxide. Due to the existence of electric field in gate oxide, as the holes approach the interface, some will be trapped, forming a positive oxide-trap charge. It is believed that hydrogen ions (protons) are likely to be released as holes “hop” through the oxide or as they are trapped near the Si/Oxide interface. The hydrogen ions can also drift to the Si/Oxide where they may react to form interface trap charges [5]. The threshold voltage is affected by both of the above charges. The radiation-induced defect densities are quantitative representations of trapped charge integrated across the thickness of the oxide (N_{ot}), and the number of interface traps at the semiconductor/oxide interface (N_{it}), which can be obtained as follows [14]:

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