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A unified analytical drain current model for Double-Gate Junctionless Field-Effect Transistors including short channel effects

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ABSTRACT

In this paper, a unified analytical model for the drain current of a symmetric Double-Gate Junctionless Field-Effect Transistor (DG-JLFET) is presented. The operation of the device has been classified into four modes: subthreshold, semi-depleted, accumulation, and hybrid; with the main focus of this work being on the accumulation mode, which has not been dealt with in detail so far in the literature. A physics-based model, using a simplified one-dimensional approach, has been developed for this mode, and it has been successfully integrated with the model for the hybrid mode. It also includes the effect of carrier mobility degradation due to the transverse electric field, which was hitherto missing in the earlier models reported in the literature. The piece-wise models have been unified using suitable interpolation functions. In addition, the model includes two most important short-channel effects pertaining to DG-JLFETs, namely the Drain Induced Barrier Lowering (DIBL) and the Subthreshold Swing (SS) degradation. The model is completely analytical, and is thus computationally highly efficient. The results of our model have shown an excellent match with those obtained from TCAD simulations for both long- and short-channel devices, as well as with the experimental data reported in the literature.

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1. Introduction

As the size of the conventional MOSFETs is reduced down to the nanoscale domain, the scaling issue is becoming much more challenging due to several technological and manufacturing process issues. Ultra-sharp source and drain (S/D) junctions are required in devices having very small channel length, to prevent the spreading of the source/drain dopants into the channel region. This causes an increase in the leakage current of the device. Also, in order to achieve this type of junctions, more advanced lithographic and annealing technologies have to be employed, which leads to an increase in the overall manufacturing cost of the chips. To alleviate this problem, a novel device structure was proposed by Collinge et al. [1], which does not need any junction, and is termed as the Junctionless Field-Effect Transistor (JLFET).

JLFETs use a simple film of silicon surrounded by an electrically isolated metal or poly-silicon that acts as a gate to control the flow of electrons through the film [2]. The film is heavily doped n-type (n-channel), which renders it to behave like a conductor. The gate modulates the flow of electrons between source and drain by changing the depletion level of the film under the gate. The structure of JLFETs is simple enough so that it can be cheaply produced even at very small sizes, thus having the potential to lead to a technology that would produce cheaper FETs in the near future. The doping of the channel is very high, hence, it is very difficult to turn the device off with a single gate; hence, more than one gate are used for good electrostatic control over the channel [3].

In this work, a symmetric Double-Gate structure is considered with its schematic as shown in Fig. 1. In Double-Gate JLFETs (DG-JLFETs), a film of silicon is sandwiched between two gates with oxide layers in between, having equal thickness and work function. The two gates are connected to each other and held at the same potential, with the resulting structure being referred to as a symmetric one. The Double-Gate structure, having different oxide thickness, and/or different work functions of gates, and/or with gates held at different potentials, is referred to as an asymmetric structure.

A portion of the film under the gates acts as the channel region, while the parts of the film outside it are the source and drain regions. The bias voltages are applied at the drain (V_{DS}) and gate (V_{GS}) terminals, both with respect to the source terminal, which is grounded. An acceptable value of the threshold voltage can be achieved by properly choosing the difference between the work functions of the gate and the semiconductor. Typically, gate material with high work function is chosen, because of which metals

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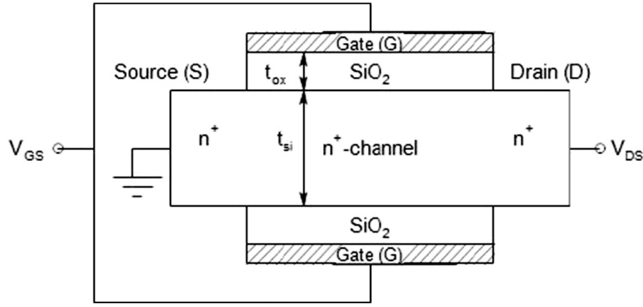

Fig. 1. The schematic of a symmetric Double-Gate (DG) n-channel JLFET: t_{ox} and t_{Si} are the thickness of SiO_2 and the channel respectively.

like Platinum (Pt – 5.65 eV) or p^+-poly is used as the gate material. In this work, we have chosen the latter.

Accurate analytical modeling of JLFETs has become very important of late, because of the need for fast simulation of circuits employing such devices. Several models have been reported in the literature for long channel JLFETs [4–6]. An analytical model for the drain current of long channel DG-JLFETs has been reported by Duarte et al. [4], in which they have represented the main physical characteristics for the drain current of the device that flows in the bulk. However, they have adopted a piece-wise approach, which may cause convergence problems in compact modeling. Only bulk conduction mechanism is considered in this model, which may not be valid for gate voltage greater than the flatband voltage.

In order to avoid the discontinuity in the model, a continuous charge based model has been reported by the same group of authors [5] for symmetric long channel DG-JLFETs. It is based on Pao-Sah electrostatic assumptions [6], and has been developed by extending the parabolic approximation of the channel potential in the subthreshold and linear regions. In the Pao-Sah integral, this parabolic channel potential was also extended to the accumulation region, where it failed to capture the correct device behavior, since in this region, the transport mechanism changes significantly from bulk conduction to surface conduction, with a different value for the carrier mobility (surface as against bulk).

A charge-based model is reported by Sallese et al. [7], which includes the surface conduction mechanism, and is based on the linearization of the electric potential, and application of a finite difference method for the solution. It is continuous all through the different regions of operation; however, it uses numerical integration, which is not practical for compact modeling [8]. Also, consideration of field dependence of mobility is missing in all the works cited so far, which definitely needs to be included, if the transport is through surface conduction, which is true under accumulation.

Since JLFETs are considered for use in the nanoscale domain, hence, it is necessary for the developed models to include various short channel effects that pertain to these devices, namely Drain-Induced Barrier Lowering (DIBL), Subthreshold Swing (SS) degradation, etc. Inclusion of short-channel effects through numerical simulations has been reported [9,10]. Other models [11,12] have been proposed, based on a decomposition of the Poisson's equation into its 2D and 1D parts, and use of the conformal mapping technique.

Another model has been reported for DIBL and SS by solving the 2D Poisson's equation using a variable separation technique [13] to extract the 2D potential distribution in the channel, and then using this, an analytical model for the subthreshold current in nanoscale DG-JLFETs is derived. There is another reported work [14], which solves for the potential distribution in the channel by splitting the 2D Poisson's equation into a 1D Poisson's equation and a 2D Laplace equation. However, based on this approach, it is still impossible to extract an explicit expression for the subthreshold current and its slope.

Other interesting works have also been published in the literature, that are based on 2D Poisson's equation [15], conformal mapping technique and Lambert's W-function [16]. A charge-based model, considering both depletion and accumulation, has been presented in [17]. A very recent paper [18] presented a model for triple-gate junctionless nanowire transistors, considering the effect of fin height and width on the device capacitance, and thus, on the potential and charges. All these works [15–18] also dealt with various short channel effects, viz. mobility degradation, threshold voltage roll-off, DIBL, CLM, series resistance, velocity saturation, etc.

In this work, we have developed a simple and analytical unified model for DG-JLFETs, by separating its operation into four modes: subthreshold, semi-depletion, accumulation, and hybrid, with individual models for each of these modes. Our special emphasis has been put on the accumulation mode, which has not received adequate attention so far in the literature, and on integration of this model with the one for the hybrid mode. The piece-wise models are unified using suitable interpolation functions, thus making the overall model valid throughout the entire operating regime. It also includes the two most important short-channel effects, namely DIBL (which also accounts for the threshold voltage roll-off) and SS degradation. In Section 2, we detail the development of the model, while in Section 3, we present the results and discussion. Finally, Section 4 concludes the work.

2. Model development

Our work closely follows that reported in [19–21] for conventional MOSFETs. In Sections 2.1 and 2.2, we present the models for the subthreshold and semi-depleted modes of operation. Our proposed model for the accumulation mode is discussed in Section 2.3, and in Section 2.4, we present the integration of this model in the hybrid mode. The unification technique for these various models is developed in Section 2.5. Finally, in Section 2.6, the inclusion of the short-channel effects in the model is discussed.

2.1. Subthreshold mode

For gate voltage (V_{GS}) less than the threshold voltage (V_{TH}), the whole channel region gets fully depleted. Ideally, there should not be any current flow, since there is no neutral channel under this condition. However, the mobile carriers present in the source/drain regions, can surmount the source/drain-channel potential barrier, and appear in the channel. Since the barrier heights at the two junctions are different (note that the barrier at the source side is less than that at the drain side, due to the application of the drain voltage V_{DS}), a carrier concentration gradient appears across the channel, resulting in a diffusion current, given by [5]:

$$I_{DS} = \mu_b \phi_t (W/L) \sqrt{2\pi q \varepsilon_s \phi_t N_D} \exp[(V_{GS} - V_{TH})/\phi_t] \times [1 - \exp(-V_{DS}/\phi_t)] \quad (1)$$

where μ_b is the carrier bulk mobility, ϕ_t (=kT/q, with k being the Boltzmann's constant, T is the absolute temperature, and q is the Coulomb charge) is the thermal voltage, W and L are the width and length respectively, ε_s is the permittivity of Si, N_D is the channel doping density (same as that of source/drain), and V_{TH} is the long-channel threshold voltage, expressed as [5]:

$$V_{TH} = V_{FB} - [qN_D t_{Si}^2/(8\varepsilon_s)][1 + 4\varepsilon_s/(C'_{ox} t_{Si})] \quad (2)$$

where V_{FB} is the flatband voltage, and C'_{ox} (= ε_{ox}/t_{ox}, with ε_{ox} being the permittivity of SiO_2) is the oxide capacitance per unit area. It is to be noted that Eq. (1) is valid only for $V_{GS} < V_{TH}$, and for

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