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X-band 5-bit MMIC phase shifter with GaN HEMT technology

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ABSTRACT

The design approach and performance of a 5-bit digital phase shifter implemented with 0.25 μm GaN HEMT technology for X-band phased arrays are described. The switched filter and high-pass/low-pass networks are proposed in this article. For all 32 states of the 5-bit phase shifter, the RMS phase error less than 5.5°, RMS amplitude error less than 0.8 dB, insertion loss less than 12 dB and input/output return loss less than 8.5 dB are obtained overall 8–12 GHz. The continuous wave power capability is also measured, and a typical input RF P_{1dB} data of 32 dBm is achieved at 8 GHz.

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1. Introduction

Many communication and radar systems are based on phased-array antennas for achieving electronic beam control and fast beam scanning, such as collision avoidance, the global positioning system (GPS) and active phased array antennas (APAAs) [1,2]. The current available solid-state phase shifters, the PIN diode and GaAs FET, have their limitations. The PIN diode phase shifter can handle high power, but it draws significant DC current when the diodes conduct. Although the GaAs FET phase shifter draw very low DC current, they have limited RF power handing capability [3]. The research into wide-bandgap semiconductors has progressed significantly over the last few years. High breakdown voltages (~100 V) and high current densities (~1.5 A/mm) are achieved for the GaN HEMT devices [4]. Therefore, the GaN HEMT-based phase shifter owns very high power handing capability and can offers higher operation reliability, especially in the radiation and high temperature environment.

Among the different topologies for phase shifter, the loaded-line phase shifter is the best choice for differential phase values $\Delta\Phi$ smaller than 45° for its sample structure. However, the loaded-line phase shifter always occupies a relatively large chip area especially in a low operating frequency. In addition, the operating bandwidth is narrow for its poor phase accuracy. For the switched-filter topology, the FET switches are directly integrated into the filters, and the FET parasitic capacitances can be absorbed into the filter network, which achieves relatively flat phase shift versus frequency characteristics and small chip size. The high-pass/low-pass phase shifter has been found to be an ideal architecture for the advantage of large phase shift values and the high-pass/low-pass topology is suitable for many applications due to its relatively flat broadband phase response and its ability to cancel out phase effects from switches and routing schemes [5–8].

Recently, several GaN HEMT-based phase shifters based on high-pass/low-pass or switched-filter has been reported, but limited to the 1-bit phase shifters [9–12]. In this article, an X-band digital 5-bit MMIC phase shifter has been presented with 0.25 μm GaN HEMT technology. The phase shifter monolithic microwave integrated circuit (MMIC) provides 32 phase shift states between 0° and 360° in increments of 11.25°. Finally, the digital 5-bit phase shifter is presented with good input return loss, low RMS phase error, low RMS amplitude error and high power handing capability within the design bandwidth.

2. Circuit design

The switched filter is proposed for 11.25° and 22.5° phase bit to reduce the area of chip and improve the phase shift accuracy and the other degree phase bit of 45°, 90° and 180° is based on high-pass/low-pass filter networks. To minimize the RF signal leakage effect, all the gate terminals are connected to control voltage through a resistor of approximately 4 kΩ.

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The schematic of the switched filter network and its equivalent circuits are illustrated in Fig. 1.

When the switching device M_1 is pinched off and M_2 is turned on, the circuit can be thought of as the low-pass network composed of the inductors L_1, two parallel capacitors C_p, as shown in Fig. 1(b), as long as the on-state resistance R_{on2} of M_2 is quite small. The low-pass π-type filter network can be analysed by ABCD matrix with neglecting the on-state resistance of M_2, and the transmission phase can be solved as (1):

$$L_1 = \frac{Z_0 \sin\varphi}{\omega_0} C_p = \frac{\tan(\varphi/2)}{\omega_0 Z_0} \tag{1}$$

where φ is the desired phase shift, Z_0 is the characteristic impedance, and ω_0 is the centre frequency.

When the switching device M_1 is turned on, and M_2 is pinched off, the inductor L_2 is sized to parallel resonate the off-state capacitance C_{off2} of M_2 at the centre frequency of ω_0, preventing the RF signal leak to the ground. The equivalent circuit is shown in Fig. 1 (c) and the L_2 can be obtained from (2):

$$L_2 = \frac{1}{\omega_0^2 C_{off2}} \tag{2}$$

With the different control bias Vc, these two equivalent circuits in Fig. 1(b) and (c) will have a phase difference of φ at ω_0.

The high-pass/low-pass topology, which is employed in 45°, 90° and 180° circuit, consists of two single-pole/double-throw (SPDT) circuits. There are two basic two topologies for SPDTs. It can be either a series or shunt configuration. When the SPDT switch with finite isolation is used to select the high-pass/low-pass path, some amount of power will flow through the isolated path, resulting in a decrease in the amount of the absolute phase shift error [13]. The higher drain-source capacitance of the AlGaN/GaN HEMTs contributes poorer isolation for the series switch at higher frequency [3]. Therefore, the shunt configuration is adopted for the SPDT. In order to improve the insertion loss and the isolation performance, a λ/4 transmission line can be placed between the common port and the shunt HEMT. The impedance and the length of the λ/4 transmission lines are optimized with the circuit simulator for the best insertion loss and isolation and the gate width of shunt HEMTs are optimized as well. Fig. 2 shows the SPDT with 2 × 100 um HEMTs.

Fig.3 shows the schematic of the T-type high-pass/low-pass configuration. Through investigation of the ABCD matrices for the

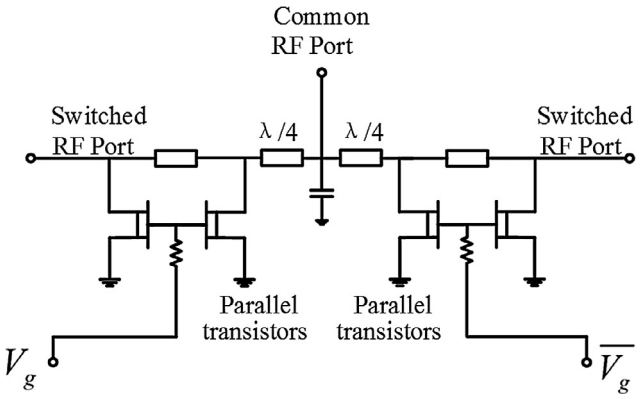

Fig. 2. The shunt configuration of AlGaN/GaN SPDT.

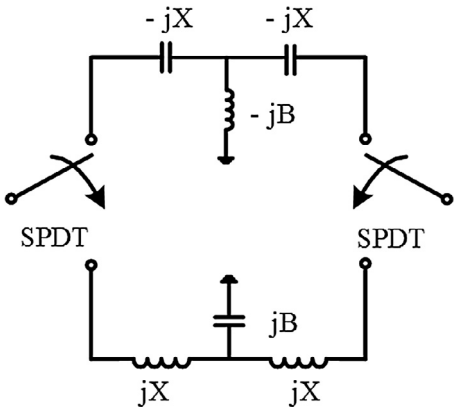

Fig. 3. The schematic of the T-type high-pass/low-pass.

networks [13], the phase shift ΔΦ caused by switching between low-pass and high-pass networks is given by:

$$\Delta\Phi = 2\arctan\frac{2B + X - XB^2}{2(1 - BX)} \tag{3}$$

The X and B are the reactance and susceptance of the T structure respectively shown in Fig.3. By assuming the phase shifter to be lossless, X and B can then be solved as

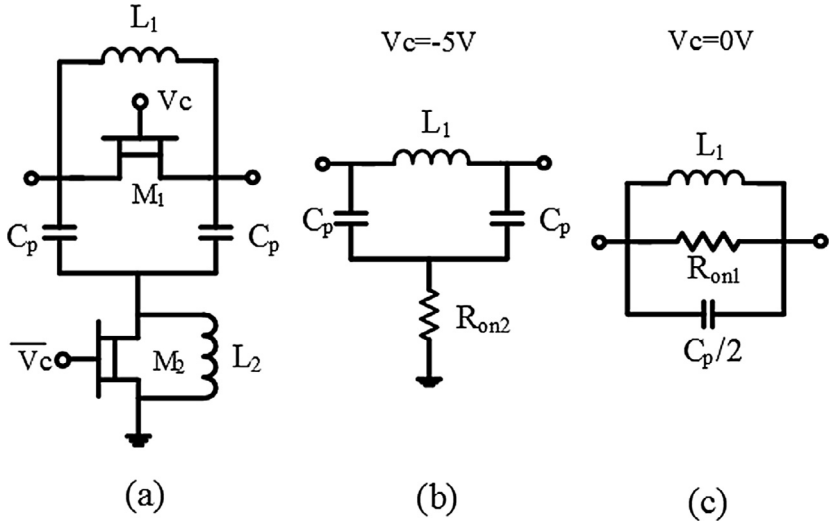

Fig. 1. (a) Topology of the switched filter. (b) Equivalent circuit when Vc = −5 V. (c) Equivalent circuit when Vc = 0 V.

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