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Temporal and voltage stress stability of high performance indium-zinc-oxide thin film transistors

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ABSTRACT

Thin film transistors (TFTs) based on transparent oxide semiconductors, such as indium zinc oxide (IZO), are of interest due to their improved characteristics compared to traditional a-Si TFTs. Previously, we reported on top-gated IZO TFTs with an *in-situ* formed HfO_2 gate insulator and IZO active channel, showing high performance: on/off ratio of $\sim 10^7$, threshold voltage V_T near zero, extracted low-field mobility $\mu_0 = 95\ cm^2/V{\cdot}s$, and near-perfect subthreshold slope at 62 mV/decade. Since device stability is essential for technological applications, in this paper we report on the temporal and voltage stress stability of IZO TFTs. Our devices exhibit a small negative V_T shift as they age, consistent with an increasing carrier density resulting from an increasing oxygen vacancy concentration in the channel. Under gate bias stress, freshly annealed TFTs show a negative V_T shift during negative V_G gate bias stress, while aged (>1 week) TFTs show a positive V_T shift during negative V_G stress. This indicates two competing mechanisms, which we identify as the field-enhanced generation of oxygen vacancies and the field-assisted migration of oxygen vacancies, respectively. A simplified kinetic model of the vacancy concentration evolution in the IZO channel under electrical stress is provided.

1. Introduction

Over the past decades, transparent amorphous oxide semiconductors (AOSs)—such as In-Zn-O (IZO) and In-Ga-Zn-O (IGZO)—have been widely studied as superior materials in making high-performance thin film transistors (TFTs). Compared to traditional amorphous silicon, AOSs have shown high field-effect mobility, high transparency in the visible wavelength region, room-temperature deposition capability on arbitrary substrates, high surface planarity, controllable carrier density and acceptable threshold voltage stability [1–7]. These superior characteristics have made AOSs very attractive for the display industry, where one type of AOS (IGZO) is already industrialized in making TFTs for backplane applications of active matrix organic light-emitting diodes (OLEDs). The need for practical application in display industry requires AOS TFTs to have stable characteristics, with threshold voltage V_T, on-state current I_{ON}, and on/off ratio I_{ON}/I_{OFF} remaining relatively unaffected due to aging, electrode biasing or environmental exposure. Several research groups have studied the V_T stability of IZO and IGZO TFTs under V_G gate bias stress [8–14] with varying results due to the complex mechanisms involved. The stability of the threshold voltage V_T in AOSs TFTs can depend on stress time and the magnitude of the V_G-induced electric field [8–15], AOS channel deposition technique and TFT structure [13,14], ambient atmosphere [11,12], thickness of the channel material [9] and different passivation materials [15]. Generally speaking, longer stress times and larger V_G-induced electric fields yield larger V_T shifts. These shifts could be related to creation of defect states near channel/dielectric interface [4] or the trapping of charges in the dielectric layer [4,8,10], which further depend on the quality of dielectric layer. A passivation layer is known to improve TFT stability because AOS material may be sensitive to ambient atmosphere [15], with reports of hydrogen/water and oxygen shifting transfer curves in opposite ways during gate bias stress [11,12]. Due to these complications, when measuring threshold stability in amorphous material, researchers often use empirical power-law or stretched-exponential equations to fit experimental data [16].

In this paper, we will report on both the temporal and the voltage stress stability of our high-performance of top-gated IZO TFTs with a HfO_2 dielectric gate insulator. We find that as our IZO TFTs age (in darkness at room temperature), they exhibit a V_T shift towards negative voltages, indicative of increasing oxygen vacancy concentration in the IZO channel material (where oxygen vacan-

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cies are the primary donor species [17]). Then voltage stress stability of IZO TFTs is investigated, where two different directions of V_T shift under negative V_G stress are observed on freshly-annealed TFTs and aged TFTs, indicating two different competing mechanisms. Based on experimental results, we identify these two mechanisms as the field-assisted creation of oxygen vacancies (increasing channel doping and making the channel more difficult to deplete, leading to a negative V_T shift) and field-induced migration of positively-charged oxygen vacancies towards the top interface (leading to a positive V_T shift). A preliminary theoretical analysis of both mechanisms, consistent with the experimental data, will be provided later in this paper.

2. Fabrication

The fabrication processes for TFTs shown in Fig. 1(a) and (b) are similar since they have similar structures. For the first structure in Fig. 1(a), the detailed fabrication process follows our previous publication [18]. To further reduce gate leakage and improve gate dielectric material reliability, an additional layer of high quality HfO_2 can be deposited between e-beam deposited HfO_2 and top gate contact by atomic layer deposition (ALD). This modified structure of IZO TFTs is shown in Fig. 1(b). For both types of devices we started with a silicon wafer coated with 500 nm thermally grown SiO_2, on top of which we deposited 20 nm of IZO sputtered from a 90 wt.% In_2O_3-10 wt.% ZnO target by dc magnetron sputtering at room temperature. During IZO deposition, the distance between sputter target and silicon wafer was 10 cm; the dc bias was 280 V with a power density of 0.22 W/cm^2; the ambient gas flow was kept at a volume ratio Ar/O_2 = 86/64. Then, the IZO active channel was patterned by using conventional photolithography, followed by dilute HCl etching. After IZO active channel deposition, the source and drain metal electrodes were patterned by photolithography and lift-off: the contact metal stack was 50 nm Mo, 10 nm Cr and 100 nm Au, sequentially deposited by e-beam evaporation. After that, Hf metal was deposited on gate area using the same e-beam evaporation technique, while there was a small oxygen flow at ~1 sccm and relatively high chamber pressure of $\sim 2 \times 10^{-5}$ Torr. Due to the existence of oxidants in the chamber, after Hf deposition, there was a 16 nm partially oxidized layer of HfO_x on top of IZO. Then, in the case of devices of Fig. 1(b), an additional 24 nm layer of HfO_2 was deposited by using ALD from a Hf(N$(CH_3)_2)_4$ precursor at 200 °C within 2 h, to provide a better gate dielectric insulator stack as well as a passivation layer for the exposed IZO layer between the top gate and source/drain electrodes. Finally, a photolithographically-defined top-gate electrode consisting of 10 nm Cr and 70 nm Au was deposited by e-beam evaporation and lifted off. The final TFTs had width W = 200 μm and gate lengths L_G = 50, 100, or 150 μm.

As described in our previous publication [18], the TFTs show transistor characteristics only after annealing for 4 h at 300 °C in air, because before annealing, those TFTs do not have a sufficiently good dielectric/IZO interface to permit gate control of the carriers in the IZO channel. Annealing allows the partially oxidized layer of HfO_x to react with the IZO channel to form a fully oxidized HfO_2 insulator layer in the near-interface region. This reaction-formed interface has been shown [18] to provide a high interface quality and excellent device results. The reaction and formation of HfO_2 at the gate/channel interface is predicted, in the absence of kinetic constraints, by the negative free energy of reaction between Hf metal and indium oxide ($\Delta G = -807.6$ kJ/mol at 200 °C) [19].

After annealing, both types of IZO TFTs were characterized by using a Hewlett-Packard multi-frequency LCR meter (model 4275A, to measure capacitance) and Agilent 4155C semiconductor parameter analyzer (to measure current-voltage characteristics). In addition to room-temperature measurements, the TFTs were also measured as a function of temperature in the T = 200–350 K range by using a variable-temperature cryostat.

3. Experimental results

The TFT characteristics were measured using a semiconductor parameter analyzer in a light-tight box with the substrate grounded. Fig. 2(a) shows the transfer curves of TFTs without additional ALD-deposited HfO_2 passivation, as in Fig. 1(a), measured 15 days after annealing in air, showing an on/off ratio about 10^7, with no apparent threshold shift between the two curves at different drain voltage (V_D = 0.1 and 1.0 V). Instead of estimating the saturation mobility, often reported in TFT characterization [20], we use the Y-function to calculate a more reliable low-field channel mobility μ_0 [21]:

$$Y = \frac{I_D}{\sqrt{g_m}} = \sqrt{\frac{W}{L_G}\mu_0 C_{ox} V_D (V_G - V_T)} \quad (1)$$

where $g_m = \partial I_D / \partial V_G$ is the transconductance, μ_0 is the low-field mobility, and C_{ox} is the gate capacitance per unit area. The estimated threshold voltage is $V_T = -0.02$ V and low field mobility is $\mu_0 = 95$ cm^2/V·s. The subthreshold slope is remarkably small: SS ~ 62 mV/decade, close to the room temperature theoretical limit of $2.3 k_B T/e$ = 60 mV/decade. The corresponding transistor characteristics of devices with an added ALD-deposited HfO_2 layer, shown in Fig. 1(b), are presented in Fig. 2(b). Again, we observe excellent transistor characteristics, with SS ~ 67 mV/decade. The measured

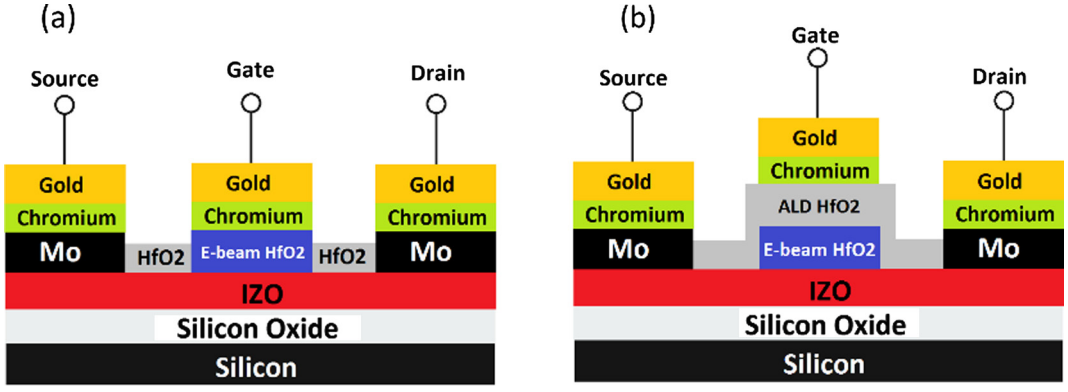

Fig. 1. Schematic cross sectional view of IZO TFTs with e-beam deposited and *in-situ* reacted HfO_2 gate dielectric without (a) and with (b) an additional ALD-deposited HfO_2 layer underneath the gate electrode.

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