Solid-State Electronics 136 (2017) 75–80

Contents lists available at ScienceDirect

Solid-State Electronics

journal homepage: www.elsevier.com/locate/sse

Design strategies for ultra-low power 10 nm FinFETs

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ARTICLE INFO

Article history:
Available online 20 June 2017

The review of this paper was arranged by A. A. Iliadis, A. Akturk, R. P. Tompkins, and A. Zaslavsky

Keywords:
FinFET
3D TCAD
GIDL
Ultra-low power

ABSTRACT

In this work, new design strategies for 10 nm node NMOS bulk FinFET transistors are investigated to meet low power (LP) (20 pA/μm < I_{OFF} < 50 pA/μm) and ultralow power (ULP) (I_{OFF} < 20 pA/μm) requirements using three dimensional (3D) TCAD simulations. The punch-through stop implant, source and drain junction placement and gate workfunction are varied in order to study the impact on the OFF-state current (I_{OFF}), transconductance (g_m), gate capacitance (C_{gg}) and intrinsic frequency (f_T). It is shown that the gate length of 20 nm for the 10 nm node FinFET can meet the requirements of LP transistors and ULP transistors by source-drain extension engineering, punch-through stop doping concentration, and choice of gate workfunction.

1. Introduction

Tri gate FinFET devices have already replaced conventional planar MOSFETs for 14 nm and beyond due to their superior control over the channel, resulting in lower values of subthreshold swing (SS) and drain induced barrier lowering (DIBL). Bulk FinFETs minimize the problems related to FinFETs on silicon on insulator (SOI) such as higher wafer cost and poor heat dissipation. In addition, gate induced drain leakage (GIDL) is found to be a limiting factor in achieving ultralow values (<100 pA/μm) of OFF-state current (I_{OFF}). There are several studies which offer approaches to reduce GIDL current in FinFET devices [1,2]. The I_{OFF} can be lowered by increasing the threshold voltage of the transistor. This can be achieved by multi-threshold voltage techniques such as engineering source-drain extension regions, tuning gate workfunction and by increasing the gate length [3,4]. Longer gate length enables lower leakage and mitigates short channel effects (SCEs) for LP and ULP transistors, however, requires more device area [5]. In addition, it tends to degrade analog figure of merit (FOM) such as cut-off frequency, $f_T = g_m/2\pi C_{gg}$ where Cgg is the total gate capacitance. This is because transconductance decreases and C_{gg} increases with increase in the gate length.

Different techniques have been proposed such as HALO implant and graded channel design to overcome the degradation of FOM. In nanoscale devices, enabling these techniques poses technological challenges. The concept of source-drain engineering (also known as gate-source-drain overlap) has been studied to overcome short channel effects (SCEs) and lowering OFF-state current [6–8]. Prior research on multi-threshold techniques has mainly focused on SOI FinFETs. In this work, aforementioned three techniques have been explored for bulk FinFETs to meet the I_{OFF} requirements of LP and ULP transistors.

2. Device simulation

The International Technology Roadmap for Semiconductors (ITRS) projected fin width and gate length for FinFETs extending to 7 nm node are illustrated in Fig. 1. Beyond 7 nm FinFETs, new transistor architectures such as vertical gate-all-around FETs (VGAA) and monolithic 3D CMOS (M3D) are just a few of the future candidates [9]. This study is carried out for bulk silicon n-channel FinFETs matching the ITRS requirements for 10 nm node.

The device parameters for simulations are listed in Table 1. The gate length is 20 nm and an equivalent gate dielectric thickness (EOT) is 0.8 nm. The source-drain doping of 1.5×10^{20} cm^{-3} is used. A channel stop implant has been created with a doping level ranging from 1×10^{17} cm^{-3} to 5×10^{18} cm^{-3}. Fig. 2 shows the device constructed for simulations.

Three-dimensional process and device simulations of tri-gate FinFETs were performed using Silvaco 3D VictoryProcess and VictoryDevice process and device simulators [10]. FinFETs are created using deposition, etching, diffusion, and Monte-Carlo implantation

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http://dx.doi.org/10.1016/j.sse.2017.06.012
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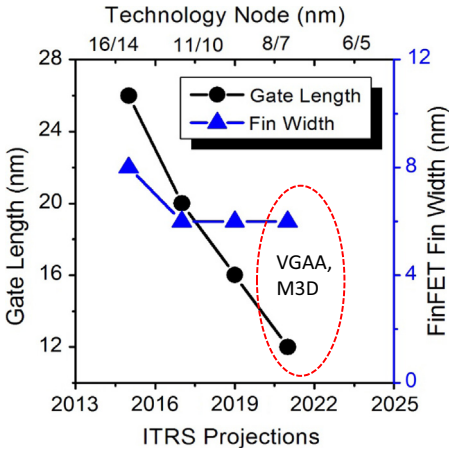

Fig. 1. Projected fin width and gate length for upcoming technology nodes [9].

Table 1
Parameters used for FinFET simulations.

Parameters	Value
Gate length	20 nm
Fin height (H_{fin})	40 nm
Fin thickness (W_{fin})	6 nm
Gate oxide thickness (EOT)	0.83 nm
Source/Drain doping	1.5×10^{20} cm^{-3}

modules of VictoryProcess. The device simulations employed use the Bohm Quantum Potential (BQP) model to take into account quantum confinement of carriers in three dimensions [11]. The mobility in the surface channel is modeled using the 'CVT' model that takes into account the effects of transverse and longitudinal fields [12]. Other effects such as Auger and concentration dependent Shockley-Read-Hall recombinations are also included in simulations. Hurkx model with its band-to-band tunneling (BTBT) formulation has been incorporated to analyze GIDL. The BTBT generation rate G_{BTBT} is given by

$$G_{BTBT} = A \cdot \exp\left(\frac{-B}{E}\right) \cdot \left(\frac{E}{E_1}\right)^{P} \quad (1)$$

where E is the transverse electric field, $E_1 = 1$ V/cm; $P = 2.5$ for phonon assisted BTBT transition as silicon is an indirect semiconductor. A and B are Kane's parameters for silicon given as $A = 4 \times 10^4$ cm^{-3} s^{-1} and $B = 1.9 \times 10^7$ V/cm [13]. The simulated I_{DS}-V_{GS} characteristics obtained are shown in Fig. 3 and compared with the reported experimental data of a 20 nm bulk FinFET [14] validating the models used.

Using these models, various methods to meet the targets for LP and ULP 10 nm node NMOS FinFET transistors have been investigated.

3. Results and discussion

In this section, the impacts of punch-through doping, source and drain extension engineering, and gate workfunction on the I_{OFF} and transconductance are investigated and results are discussed below.

3.1. Impact of Punch-through stop doping (PTS)

The effect of PTS doping on the leakage current in bulk FinFETs has been studied by Manoj et al. [15]. It is well known that threshold voltage of an n-type (or p-type) MOSFETs can be increased by increasing p-type (n-type) doping in the channel. The introduction of dopant also results in mobility degradation. In order to reduce the impact on the mobility, a retrograde profile is used in this study. The threshold voltage is changed by changing the dose of punch-through stop (PTS) implant wherein the peak of the implant is located below the fin. However, due to the tail of PTS implantation, the channel region does not remain completely undoped.

In order to evaluate leakage performance, the p-type PTS doping is changed from 1×10^{17} cm^{-3} to 4×10^{18} cm^{-3}. These simulations are done for a gate workfunction (WF) of 4.5 eV. A higher fin body doping results in lower OFF-state current and reduced transconductance because of mobility degradation (Fig. 4(a)). Transconductance is extracted in the saturation regime. Effect of body doping on SS and DIBL is shown in Fig. 4(b). DIBL is extracted using $DIBL = (V_{th,sat} - V_{th,lin})/(V_{DS,sat} - V_{DS,lin})$. Where $V_{th,sat}$ and $V_{th,lin}$ are the threshold voltage values at saturation and linear mode respectively. $V_{DS,sat}$ is 0.75 V and $V_{DS,lin}$ is 0.05 V. DIBL and SS are improved by increasing PTS doping. It is clear that adjusting PTS doping can achieve lower DIBL and SS, but also lowers transconductance and I_{OFF} is not reduced enough to meet the requirements for ULP transistors.

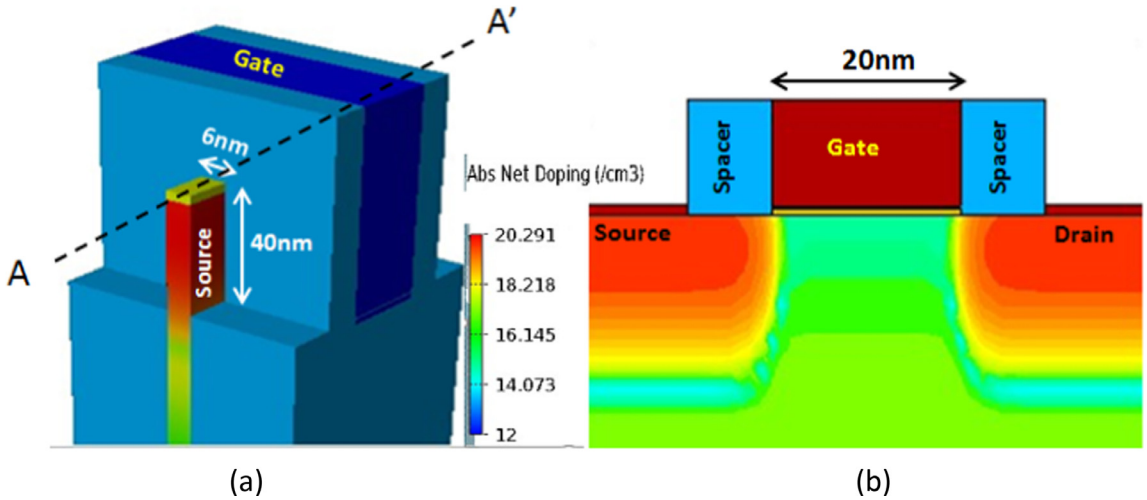

Fig. 2. (a) Structure of the 3D nFinFET modeled in this work; (b) cross section along AA' showing source-drain and channel doping concentrations labeled in logarithmic scale.