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Process modules for GeSn nanoelectronics with high Sn-contents



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ABSTRACT

This paper systematically studies GeSn n-FETs, from individual process modules to a complete device. High-k gate stacks and NiGeSn metallic contacts for source and drain are characterized in independent experiments. To study both direct and indirect bandgap semiconductors, a range of 0–14.5 at.% Sn-content GeSn alloys are investigated. Special emphasis is placed on capacitance-voltage (C-V) characteristics and Schottky-barrier optimization. GeSn n-FET devices are presented including temperature dependent I-V characteristics. Finally, as an important step towards implementing GeSn in tunnel-FETs, negative differential resistance in Ge_{0.87}Sn_{0.13} tunnel-diodes is demonstrated at cryogenic temperatures. The present work provides a base for further optimization of GeSn FETs and novel tunnel FET devices.

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1. Introduction

Recently, GeSn alloys have emerged as promising group IV semiconductors for electronic [1] as well as photonic [2,3] applications. The breakthrough in epitaxial growth of high-Sn content and strain relaxed layers, enabled fundamental direct bandgap group IV alloys grown on Si [4,5]. The direct bandgap property is a requirement for efficient Si based light emitters. However, such alloys may also serve as performance boosters in nanoelectronics. The small effective mass and associated reduction of intra-valley scattering yields high mobility Γ -electrons. Performance of GeSn based n-type Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) should then be superior to those of their pure Ge counterparts. In addition, the possibility of combining direct band-to-band tunneling and low bandgap should yield efficient tunnel field effect transistors (TFETs).

Mobility calculations, using the 8-band k.p method for the Γ -valley band structure and effective mass (including nonparabolicity) for the L-valley band structure, predict a significant mobility enhancement as soon as the population of Γ -valley is sufficiently large. The calculations take acoustic phonon, deformation potential, alloy disorder, ionized impurity, and inter-valley scattering into account. Modulation of the Γ -valley population

can be achieved either by changing Sn-content or layer strain. For Sn contents below ~9 at.% GeSn alloys are indirect bandgap semiconductors. Hence, the electron mobility is dominated by electrons occupying the L-valley. For larger Sn contents, above the indirect to direct bandgap transition, the Γ -valley becomes increasingly populated and the electron mobility is boosted significantly. The calculated Sn-dependent Γ -valley population and effective (weighted-average) mobility is shown in Fig. 1(a). GeSn pseudomorphically grown on Ge is Sn-content dependently biaxially compressively strained. However, growing thicker GeSn layers leads to strain relaxation or even tensilely strained GeSn when combining different Sn-contents [6,7]. Decreasing compressive strain has the same effect as increasing Sn content, leading to an increase of Γ -valley population and of Γ -electron mobility according to Fig. 1(b). In contrast, L-electron mobility is of the order of 4×10^3 cm²/V s for all Sn-contents and strain values presented here. The large difference between Γ - and L-electron mobility comes from a much larger effective mass of the L-electrons. However, just above the indirect to direct transition, the Γ -electron mobility is still limited by strong inter-valley Γ -L scattering, which gives a large relative contribution to total scattering due to a large L-valley density of states (while the L-electrons are less affected, because of a smaller density of states of Γ). Together with a small fraction of Γ -electrons, this implies that in alloys with 8.5 at.% Sn, at the direct to indirect transition, the mobility is always dominated by the L-electrons. However, when Γ -L spacing increases,

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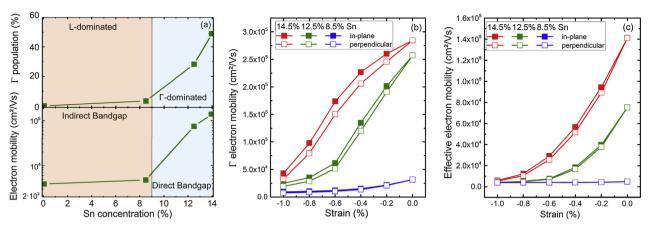


Fig. 1. (a) Calculated Γ -valley population (top) and effective electron mobility, at 300 K and 10¹⁴ cm⁻³ electron density, vs Sn-content (bottom) at zero strain. (b) Γ and (c) effective electron mobilities for various GeSn alloys, dependent on biaxial strain.

by decreasing strain or increasing Sn-content, inter-valley scattering is reduced, and Γ -population becomes significant. Consequently, not only the Γ -electron mobility but also the effective electron mobility, displayed in Fig. 1(c), strongly increases. It is also worth noting that biaxial strain induces a non-negligible anisotropy of the Γ -valley, and in case of compressive strain the inplane mobility, relevant for MOSFETs, is larger (by up to \sim 20%) than perpendicular mobility.

Preliminary works on p- and n- MOSFETs [8,9] and even TFETs [10] based on GeSn alloys have been reported, however, the Sn-contents and strain values were far below the indirect to direct transition. The low solid solubility of Sn in Ge < 1 at.% and the non-equilibrium growth restricts the thermal budget to temperatures <350 °C for Sn-contents above 10 at.% making process integration challenging.

In this work we discuss advances on low temperature process modules for GeSn-FET devices with Sn-contents up to 13 at.%, including high-k/metal gate stack deposition and low resistivity metallic NiGeSn contact formation. Emphasis is placed on the fabrication and characterization of metal-semiconductor-metal (MSM) diodes for Schottky-barrier height (SBH) extraction and Schottky-barrier tuning by dopant segregation (DS). GeSn n-FETs are fabricated using these modules and, as a step towards novel devices, *p-i-n* tunneling diode characterization is presented.

2. Experimental

Due to the low solid solubility of Sn in Ge (<1 at.%) growth conditions for GeSn with up to 13 at.% Sn are far from equilibrium. An industry compatible AIXTRON TRICENT RP-CVD epitaxial reactor was employed to grow these layers on 200 mm Ge buffered Si (100) wafers [11]. All process temperatures were kept below 350 °C in order to avoid Sn-diffusion and segregation. As a first key module, MOS-capacitors (MOScaps) with high-k/metal gate stacks on GeSn were investigated. After a wet HF-HCl surface preparation, 6 nm HfO2 high-k dielectric was deposited at low temperature by atomic layer deposition (ALD) followed by 40 nm sputter deposited TiN metallization both using 200 mm, industry compatible reactors. MOScaps with Sn-contents between 0 at.% (Ge-substrate) and 12.5 at.% were fabricated. Standard CMOS technology, such as photo lithography and reactive ion etching, was used to define the structures. The fabrication ended with a liftoff process after the deposition of 150 nm Al for contacts followed by forming gas annealing at 300 °C. A set of Capacitance-Voltage (C-V) characteristics at different frequencies measured on TiN/HfO₂/Ge_{0.915}Sn_{0.085} capacitors is shown in Fig. 2(a). The good GeSn/HfO₂ interface quality is evidenced by the small frequency dependent flat-band voltage shift and the small frequency dispersion in accumulation. Typical for low bandgap semiconductors, the C-V curves feature a strong minority carrier inversion response even at high frequencies >100 kHz. As a consequence, a reliable extraction of the interface state density (Dit) using the conduction method at *room temperature* becomes difficult [12]. However, the minority carrier inversion response is reduced at lower temperatures. We have thus used the *low temperature* conductance method as described in work by Nicollian and Brews [13] at T < 120 K to extract Dit values of 2×10^{12} cm⁻² eV⁻¹ at midgap for GeSn capacitors with different Sn contents (Fig. 2(b)). A study focusing on the process development and characterization of ternary SiGeSn MOScaps has been published recently [14].

A second fundamental module is contact formation. Metal-semiconductor-metal (MSM) diodes based on NiGeSn/GeSn Schottky contacts were fabricated using an oxide mask. After native oxide removal, 10 nm of Ni were deposited by sputter deposition and $\sim\!23$ nm NiGeSn was formed by rapid thermal annealing for 10 s in N₂/H₂ forming gas atmosphere. Unreacted Ni was removed by sulfuric acid (96% aq.). The van-der-Pauw method [15] has been used to measure the sheet resistance of the so formed NiGeSn films. The lowest sheet resistance was obtained by stanogermanidation at 325 °C [16]. The low-resistive NiGeSn-phase could be maintained over the complete available Sn-content range from 0 to 12.5 at.%. The sheet resistance of NiGeSn for several Sn-contents is shown in Fig. 3(d). Furthermore, a smooth NiGeSn/GeSn interface was obtained as shown by the cross-sectional Transmis sion-Electron-Microscopy (TEM) image in the inset of Fig. 3(d).

Current transport properties across a metal-semiconductor contact are determined by the Schottky-barrier. Previous studies have investigated the electron Schottky-barrier on NiGeSn/Ge_{0.958}Sn_{0.042} [17] and hole Schottky-barrier on NiGeSiSn/Ge_{0.86}Si_{0.07}Sn_{0.07} [18]. Here, we determine the NiGeSn/GeSn hole Schottky-barrier from MSM diodes with different contact areas and for several Sn-concentrations using the activation-energy method. The advantage of this method is that the electrically active contact area does not need to be known, e.g. current crowding does not affect the Schottky-barrier extraction. The temperature dependent I-V characteristics were measured in a liquid nitrogen cooled cryostat under high vacuum where the temperature range from 400 K to 100 K is covered in 10 K incremental steps. From Arrhenius plots of the current characteristics for different voltages (Fig. 3(a)) the Schottky-barrier height (SBH) was extracted. According to

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