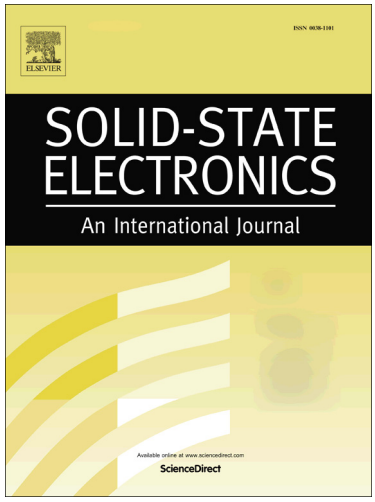

Back-gated InGaAs-On-Insulator Lateral N^+NN^+ MOSFET : Fabrication and Typical Conduction Mechanisms

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Back-gated InGaAs-On-Insulator Lateral N^+NN^+ MOSFET : Fabrication and Typical Conduction Mechanisms

H. J. Park[a*], L. Pirro[a], L. Czornomaz[b],I. Ionica[a],M. Bawedin[a], V. Djara[b], V. Deshpande[b], S. Cristoloveanu[a]
[a]IMEP-LaHC, Minatec, Grenoble INP,Univ. Grenoble Alpes, CNRS Grenoble, France
[b]IBM Research, Ruschlikon, Switzerland

***Abstract*—Back-gated InGaAs-on-insulator lateral N^+NN^+ MOSFETs are successfully fabricated by direct wafer bonding and selective epitaxial regrowth. These devices were characterized using a revisited pseudo-MOSFET configuration. Two different transport mechanisms are evidenced: volume conduction in the undepleted region of the film and surface conduction at the interface between InGaAs and buried insulator. We propose extraction techniques for the volume mobility and interface mobility. The impact of film thickness, channel width, and length is evaluated. Additional measurements reveal the variation of the transistor parameters at low temperature and under externally applied uniaxial tensile strain.**

Keywords—III-V; InGaAs; SOI; pseudo-MOSFET; MOSFET; wafer bonding; carrier mobility; strain; selective regrowth.

I. Introduction

The extension of Moore's law is based on two pillars: (i) electrostatic integrity of small transistors and (ii) improvement of transport properties for high speed. Only fully depleted devices, such as FinFETs, planar SOI or nanowires, benefit from excellent control of the gate on the channel, leading to attenuated short-channel effects and leakage current. Technology-wise, Semiconductor on Insulator (SOI)is the most straightforward, and pragmatic approach. Mobility boosters consist in adding strain, selecting the crystal orientation or, more drastically, replacing silicon with more talented semiconductors [1-5].

According to ITRS predictions [6], high-mobility channel materials such as Ge, SiGe and III-V compounds are promising candidates for the next generations of MOSFETs, able to deliver the necessary power-performance benefits and added functionality for CMOS and System-on-Chip applications [7-9]. Furthermore, devices fabricated on semiconductor-on-insulator substrates have better electrostatic control with decreased short channel effects and reduced leakage current [10-12]. Merging the merits of III-V compounds and SOI is a recent option explored as starting substrate (III-V on insulator) for device fabrication. In particular, InGaAs-on-insulator structures are attractive [13] to integrate high-performance FinFETs [14], planar MOSFETs on insulator and hybrid InGaAs/SiGe CMOS circuits [15]. This technology is rapidly evolving. Nevertheless, InGaAs-on-insulator films are prone to additional carrier scattering, compared to layers grown on bulk crystalline buffers such as InP [16] or InAlAs [17], owing to the presence of the buried oxide (BOX) and related back interface.

Our work is focused on the technological optimization via detailed investigation of transport properties in simple test devices. $In_{0.53}Ga_{0.47}As$ layers transferred on oxide were characterized using a modified version of the well-known pseudo-MOSFET (Ψ-MOSFET) configuration [18]. Lateral N^+NN^+ structures have been fabricated on InGaAs-on-insulator layers to mimic the channel transport of a MOSFET while minimizing the impact of process-induced damages. Section 2 presents the main processing steps [19]. The measurement set-up and typical transistor characteristics are shown in section 3. A suitable procedure, based on the extension of Y-function technique, is proposed in section 4 for extracting the electron mobility in the film volume and at the interface. We discuss the carrier mobility as a function of film thickness, temperature from 77K to 300K, and uniaxial tensile strain.

II. Material and Device Processing

The fabrication of back-gated lateral N^+NN^+ transistors utilizes some of the key steps developed for InGaAs FinFETs [15]. The characteristics are expected to be representative of those in fully-processed devices with back-gate operation. The n-layer is a non-intentionally doped InGaAs-on-insulator (InGaAs-OI) grown in a metal organic vapor phase epitaxial reactor. InGaAs-OI layers on Si which have an initial doping concentration of $N_D \sim 2\times10^{17} cm^{-3}$ are prepared by direct wafer bonding of nominally-undoped $In_{0.53}Ga_{0.47}As$ films of varying thickness (*25nm, 50nm, 100nm and 200nm*) grown on InP wafers as described in [20]. The carrier concentration measured by *Hall Effect* on a 200-nm-thick InGaAs on InP layer before bonding is of $2\text{-}3\times10^{16} cm^{-3}$. The buried oxide (BOX) consists of *25 nm* thermal SiO_2, *10nm* Al_2O_3 and the high-k dielectric stack used in [14], for a resulting C_{BOX} of $0.11 \mu F/cm^2$.

The fabrication of lateral N^+NN^+ structures starts with the deposition of a SiO_2 hard-mask to define the length of the n-region (Fig. 1(a)). Sn-doped $In_{0.53}Ga_{0.47}As$ N^+ regions ($N_D = 5x10^{19}\ cm^{-3}$) are selectively grown (Fig. 1(b)) at low temperature as in [21]. The hard-mask is removed (Fig. 1(c)) and a mesa isolation is performed by wet etching (Fig. 1(d)). The top interface of the n-region is formed with same high-k dielectric as used for the bottom interface. The process is completed by the deposition of a SiO_2 layer (Fig. 1(e)), etching via holes and W metal contacts (Fig. 1(f)). It should be noted that although the bottom and top InGaAs/high-k interfaces are formed with the same deposition process, they differ in the fact that the bottom interface is exposed to the thermal budget of