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Low frequency noise assessment in n- and p-channel sub-10 nm triple-gate FinFETs: Part II: Measurements and results

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ABSTRACT

Low frequency noise measurements are used as a non-destructive diagnostic tool in order to evaluate the quality of the gate oxide and the silicon film of sub-10 nm triple-gate Silicon-on-Insulator (SOI) FinFETs. It was found that the carrier number fluctuations explain the 1/*f* noise in moderate inversion for n- and p-FinFETs, which allows estimating the gate oxide trap densities. The noise spectroscopy with respect to temperature (study of the generation-recombination noise) led to the identification of the traps located in the transistors silicon film.

1. Introduction

In order to meet the ITRS specifications in terms of CMOS down-scaling, new materials, designs and structures are necessary [1]. Triple-gate FinFETs are known for their good electrostatic performances and their compatibility with CMOS processes as a continuation of Moore's law [2].

Low-frequency noise measurements can be used as a non-destructive diagnostic tool that leads to the identification of traps in the Si film and the gate oxide, thus giving information on the quality of the transistors fabrication. The study of the 1/*f* noise level with respect to the gate overdrive voltage V_{GT} leads to the identification of the 1/*f* noise origin. The study of the generation recombination (GR) noise is performed as a function of the temperature at fixed drain current. This low frequency noise spectroscopy can give access to information on the traps located in the depletion region of the transistor [3].

In this work, static and dynamic parameters have been extracted in n- and p-channel triple-gate Silicon-on-Insulator (SOI) FinFETs. Low-frequency noise has been investigated in order to determine the quality of those devices. First the main static parameters of the devices have been extracted at 300 K, then the 1/*f* noise level has been studied as a function of the gate voltage and, finally, the generation-recombination noise has been investigated in function of temperature. The theory and methodology that are useful for the parameters extraction are explained in an accompanying Part I paper [4].

2. Devices and experimental

The tested devices have been processed at imec (Belgium) for sub-10 nm technological nodes, in the framework of a comparative study between triple-gate FinFETs and gate-all-around (GAA) nanowire (NW) FETs, fabricated on SOI substrates [5]. The gate stack consists of a high-κ dielectric (HfO_2) on top of a SiO_2 interfacial layer. Each layer is 1.5 nm wide, which leads to an equivalent oxide thickness *EOT* = 1.9 nm. The gate stack is followed by EWF (TiN) and W-fill metal depositions. All tested transistors have 5 fingers of 22–23 nm height; the finger width varies from W_{fin} = 5 nm to 40 nm, which gives a total gate width going from W_m = 245 nm to 420 nm. The finger pitch is 200 nm and the gate length varies from L_m = 45 nm to 10 μm. The transistors are built on a buried oxide (BOX).

The static and noise measurements have been performed on chip using a Lakeshore TTP4 prober. The DC characteristics have been obtained with a HP 4156B. Output noise power spectral densities (PSDs) have been measured using a home-made set-up,

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which includes a low-noise transimpedance amplifier and a HP 3562A dynamic signal analyzer. This set-up allows to bias transistors by choosing the V_{GS}, V_{DS} and V_{BS} voltages. The noise spectral densities are measured from 1 Hz to 100 kHz. The input referred gate voltage noise PSD S_{VG} is obtained by dividing the measured noise voltage by the square of the measured voltage gain between the gate and the system output. This cancels the set-up bandwidth limitation.

The static parameters extraction has been performed using $I_D(V_{GS})$ characteristics at 300 K. The drain voltage has been set to V_{DS} = 20 mV so the transistors works in the linear operation regime and the bulk has been connected to the source V_{BS} = 0 V. The low frequency noise has been measured as a function of temperature from 220 K to 300 K by steps of 20 K at fixed drain current I_D. As for static measurement the linear operation regime is reached with V_{DS} = 20 mV and V_{BS} = 0 V, then the gate voltage V_{GS} was adjusted in order to set the fixed drain current from I_D = 1 μA to 5 μA by 0.5 μA steps. This paper shows the results obtained for n-channel and p-channel FinFETs with a finger width of W_{fin} = 20 nm and 30 nm.

3. Static parameters extraction

The transistors have been studied in linear operation (V_{DS} = 20 mV) at room temperature. Good behavior of the transfer DC characteristics $I_D(V_{GS})$ and $g_m(V_{GS})$ is observed for both n- and p-channels, as shown in Fig. 1.

Static parameters extraction has been further processed using the Y function method ($Y = I_D/\sqrt{g_m}$ [3]), which gives access to the threshold voltage V_{th} and the transconductance parameter $G_M = \mu_0\ C_{ox}\ W/L$. The values that will be discussed in this paper have been obtained for two iterations of the Y function method.

Once the basic DC parameters have been determined with the Y function method for different gate lengths L_m, the low-field mobility μ_0 and the access resistances R_{access} can also be extracted from a set of transistors with different gate lengths [4]. As the transconductance parameter G_M is defined by $G_M = \mu_0\ C_{ox}\ W/L$, one can write

$$\frac{1}{G_M} = \frac{L}{\mu_0 C_{ox} W} = \frac{1}{\mu_0 C_{ox} W}(L_m - \Delta L) \quad (1)$$

The low-field mobility μ_0 and the channel length reduction ΔL values can be determined from the slope and the y-intercept of $G_M{}^{-1}(L_m)$, respectively. The points corresponding to different gate lengths are shown in Fig. 2, on which a linear regression has been performed in order to estimate μ_0 and ΔL. For these n-FinFETs with W_{fin} = 30 nm, we have found that μ_0 = 259 cm^2/(V·s) and ΔL = 4.8 nm.

The effective (extrinsic) mobility attenuation factor θ_1 is defined by

$$\theta_1 = \theta_{10} + G_M R_{access} \quad (2)$$

thus the plot of $\theta_1(G_M)$ should give a straight line where the slope is equal to R_{access} and the y-intercept is equal to θ_{10}, as shown in Fig. 3. For the same n-FinFETs (W_{fin} = 30 nm), values of R_{access} = 370 Ω and θ_{10} = 707 mV have been recorded.

The values of the access resistances have been confirmed using the linear variations of the total resistance for various gate overdrive voltage V_{GT} against the gate mask length L_m. The value of the access resistance is determined at the common intersection of all lines, as shown in Fig. 4. In this case values of R_{access} = 375 Ω and ΔL = 5.5 nm have been derived, which confirms the results that have been obtained with the previously explained method.

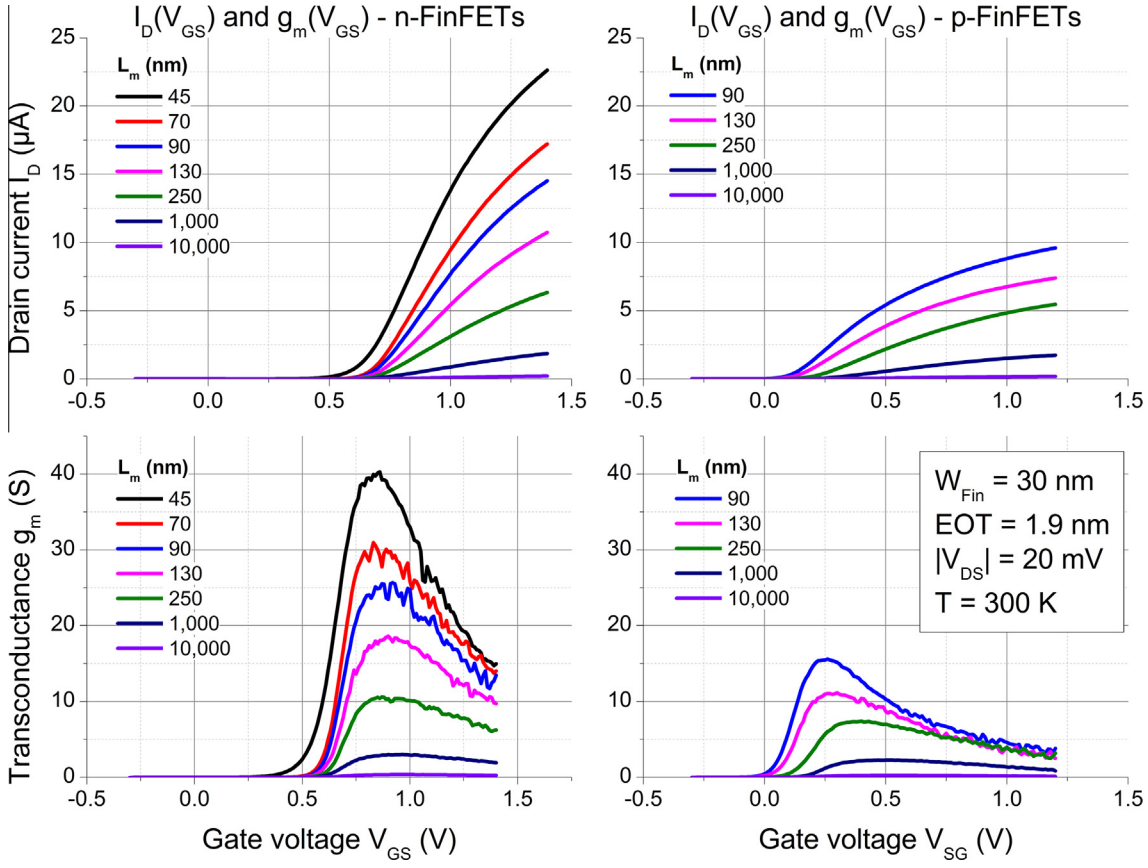

Fig. 1. Typical $I_D(V_{GS})$ and $g_m(V_{GS})$ characteristics of n- and p-FinFET for various gate lengths.

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