Solid-State Electronics xxx (2016) xxx–xxx

Contents lists available at ScienceDirect

Solid-State Electronics

journal homepage: www.elsevier.com/locate/sse

RF SOI CMOS technology on 1st and 2nd generation trap-rich high resistivity SOI wafers

B. Kazemi Esfeh [a,*], S. Makovejev [b], Didier Basso [c], Eric Desbonnets [c], V. Kilchytska [a], D. Flandre [a], J.-P. Raskin [a]

[a] ICTEAM, Université catholique de Louvain, 1348 Louvain-la-Neuve, Belgium
[b] Incize, Louvain-la-Neuve, Belgium
[c] Soitec, Parc Technologique des Fontaines, 38190 Bernin, France

ARTICLE INFO

Article history:
Available online xxxx

The review of this paper was arranged by Viktor Sverdlov

Keywords:
High-resistivity (HR) SOI substrate
Trap-rich high-resistivity silicon
Enhanced signal integrity silicon-on-insulator (eSI HR-SOI)
Substrate effective resistivity
Silicon-on-insulator
DC and RF performance
Partially-depleted (PD) SOI MOSFETs
Crosstalk
Digital substrate noise

ABSTRACT

In this work three different types of UNIBOND™ Silicon-on-Insulator (SOI) wafers including one standard HR-SOI and two types of trap-rich high resistivity HR-SOI substrates named enhanced signal integrity high resistivity silicon-on-insulator (eSI HR-SOI) provided by SOITEC are studied and compared. The DC and RF performances of these wafers are compared by means of passive and active devices such as coplanar waveguide (CPW) lines, crosstalk- and noise injection-structures as well as partially-depleted (PD) SOI MOSFETs. It is demonstrated that by employing enhanced signal integrity high resistivity silicon-on-insulator (eSI HR-SOI) compared to HR-SOI wafer, a reduction of 24 dB is measured on both generations of trap-rich HR-SOI for 2nd harmonics. Furthermore, it is shown that in eSI HR-SOI, digital substrate noise is effectively reduced compared with HR-SOI. Purely capacitive behavior of eSI HR-SOI is demonstrated by crosstalk structure. Reduction of self-heating effect in the trap-rich HR-SOI with thinner BOX is finally studied.

1. Introduction

During last decades, CMOS technology scaling-down has enabled millimeter wavelength operation and low-cost integration of digital, analog and RF systems on the same wafer for system-on-chip or system-in-package applications [1–3]. In this context, the most special advantage of SOI CMOS compared to bulk Si is the availability of high-resistivity silicon (HR-Si) substrate to achieve low crosstalk between passive and active devices and high-quality passive elements thanks to effective reduction of substrate coupling and losses in RF circuits [4,5]. However, HR-SOI substrate suffers from resistivity degradation due to the formation of parasitic surface conduction (PSC) beneath the buried oxide layer (BOX) [6–9] due to fixed oxide charges (Q_{ox}) within the oxide. One of the most efficient techniques to overcome this problem is to introduce a trap-rich layer at the Si/SiO_2 interface compatible with industrial SOI wafer production and thermal budget of standard CMOS process [8]. Such layer aims at capturing the free carriers forming the PSC and thus retaining the substrate nominal high resistivity. In this work two types of trap-rich HR-SOI wafers named 1st and 2nd generation of enhanced signal integrity (eSI HR-SOI) substrate having respectively a BOX thickness of 400 nm and 200 nm developed by Soitec are studied and compared with the classical HR-SOI substrate with a BOX thickness of 1 μm. One of the motivations of using trap-rich HR-SOI substrates with thinner BOX is the reduction of self-heating effect. Moreover, it creates a pathway for further ultimate BOX thinning used in advanced nano-scaled ultra-thin body and BOX (UTBB) fully depleted MOSFETs which allows threshold voltage control by means of back-gate biasing voltage V_{bg} [10]. Therefore, trap-rich HR-SOI with thinner BOX could be considered as a promising candidate.

2. Device description

In this work two types of trap-rich HR-SOI substrates denoted eSI Gen1 and eSI Gen2 as 1st and 2nd generations with 400 nm and 200 nm-thick BOX respectively and one standard HR-SOI with 1 μm BOX (all provided by Soitec) are characterized and compared for non-linearity effects, crosstalk, noise coupling, DC/RF figures of merit and self-heating. The test structure devices include

* Corresponding author.
E-mail address: Babak.kazemiesfeh@uclouvain.be (B. Kazemi Esfeh).

http://dx.doi.org/10.1016/j.sse.2016.10.035
0038-1101/

0.52 μm-thick CPW lines and PD SOI nMOSFETs fabricated using TowerJazz 0.18 μm SOI CMOS process (Fig. 1).

The lateral dimensions of the CPW lines are 20, 18 and 100 μm for the central conductor, slot space and ground plane, respectively. The PD SOI nMOSFETs have 145 nm-thick active silicon film with a nominal operating voltage of 2.5 V. The studied RF body-tied MOSFET has a gate length (L_g) of 0.24 μm with 16 gate fingers of 2 μm each (W_f). The studied single-finger DC nMOSFET has a gate length (L_g) of 0.26 μm with 1.5 μm width (W_f). To investigate substrate coupling we used a passive crosstalk structure consisting of two identical metallic pads embedded into RF pads for probe measurement. Active crosstalk structure is used to study the propagation of a digital noise signal through the substrate [11]. This characterization is performed by measuring the frequency spectra at the nMOSFETs drain as the output port when a square noise signal is injected in the vicinity of the nMOSFET via a metallic RF pad with a certain distance from the transistor.

3. Transistor characteristics

3.1. DC and RF performance

The DC on-wafer measurements have been done using an Agilent B1500. As shown in Fig. 2, the drain current versus gate voltage (I_D-V_G) and transconductance vs gate voltage (g_m-V_G) curves in linear regime are almost identical for the DC transistor on the 3 different wafers. To eliminate the threshold voltage variations effect and fairly compare these results, g_m/I_D ratio versus $I_D/(W/L)$ curves for the same transistors are plotted in Fig. 3.

Fig. 3 shows that similar values of maximum $g_m/I_D \sim 31\ V^{-1}$ are obtained for all substrate types, as well as similar characteristics in strong inversion, with very slight deviations in weak inversion which could be related to CMOS process and measurements variability. From Figs. 2 and 3 it can be seen that neither the existence of trap-rich layer nor the BOX thickness affects the DC characteristics of the PD SOI MOSFETs.

High-frequency measurement of studied RF body-tied nMOSFET is performed to extract the current gain cutoff frequency (f_T) as one of the major RF figures of merit. f_T is known as unity current gain frequency at which the short circuit current gain (H_{21}) becomes unity (0 dB) [12–14]. RF measurements are done in the frequency range from 40 MHz up to 40 GHz using Anristu 37369A in combination with HP4145 semiconductor-parameter analyzer. By using the off-wafer line-reflect-match (LRM) calibration technique, the reference planes at the probe tips are determined. Then by means of on-wafer dedicated de-embedding structures, the unwanted parasitic effects introduced by the RF pads are removed. H_{21} is extracted from the measured S-parameters of the transistor in saturation regime at Vg bias corresponding to the maximum of g_m [15,16]. As shown in Fig. 4, cut-off frequencies f_T on all 3 wafers are almost the same.

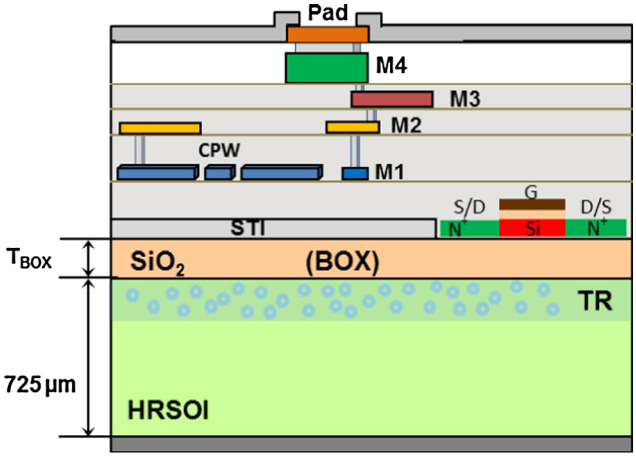

Fig. 1. Cross-section details of 4-metal layer 0.18 μm SOI CMOS process by Tower Jazz on top of high resistivity SOI substrates having different BOX thickness (T_{BOX}) provided by SOITEC.

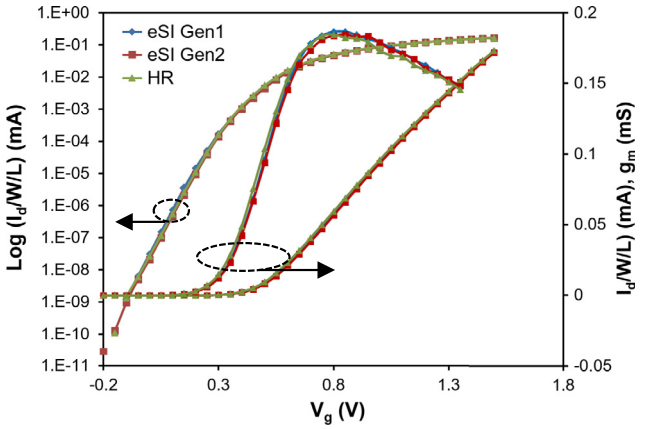

Fig. 2. Normalized I_d-V_g (linear and logarithmic) and g_m-V_g characteristics in linear regime (V_{DS} = 50 mV) of DC transistor for 3 different wafers of 1st generation of trap-rich high resistivity SOI (eSI Gen1), 2nd generation of trap-rich high resistivity SOI (eSI Gen2) and high resistivity SOI (HR).

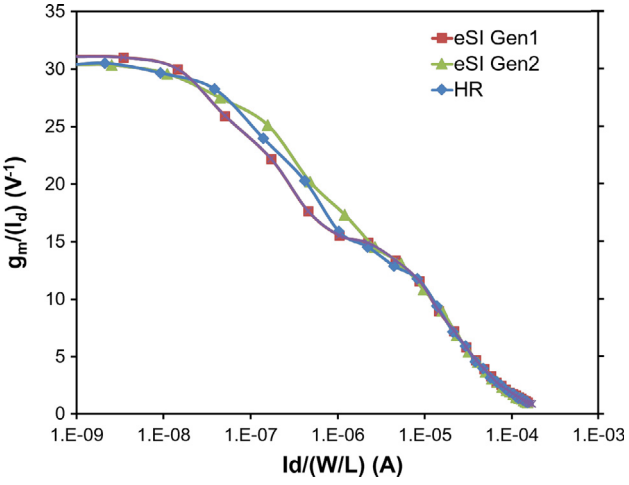

Fig. 3. g_m/I_d ratio versus $I_d/(W/L)$ DC transistor in linear regime (V_{DS} = 50 mV) on 3 different wafers of 1st generation of trap-rich high resistivity SOI (eSI Gen1), 2nd generation of trap-rich high resistivity SOI (eSI Gen2) and high resistivity SOI (HR).

According to the MOSFET small-signal equivalent circuit f_T can be in a first order expressed as [13,14,16]

$$f_T \approx \frac{g_m}{2\pi C_{gg}} \quad (1)$$

where C_{gg} is the total gate capacitance (i.e. $C_{gs} + C_{gd}$). From Eq. (1), Fig. 4 and the results of DC measurements, it can be also concluded that total gate capacitances of PD MOSFETs fabricated on three different wafers are identical.

3.2. Self-heating and coupling through the substrate

Self-heating in SOI devices becomes a critical issue because of device downscaling and use of materials with low thermal conductivity like SiO_2 [17]. Thermal conductivity of SiO_2 (1.4 $W \cdot m^{-1} \cdot K^{-1}$)

Please cite this article in press as: Kazemi Esfeh B et al. RF SOI CMOS technology on 1st and 2nd generation trap-rich high resistivity SOI wafers. Solid State Electron (2016), http://dx.doi.org/10.1016/j.sse.2016.10.035