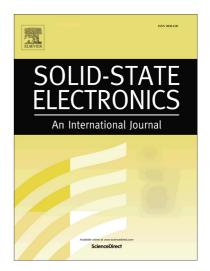
Accepted Manuscript

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PII:	S0038-1101(16)30199-X
DOI:	http://dx.doi.org/10.1016/j.sse.2016.10.032
Reference:	SSE 7129

To appear in: *Solid-State Electronics*



Please cite this article as: Šimonka, V., Nawratil, G., Hössinger, A., Weinbub, J., Selberherr, S., Anisotropic Interpolation Method of Silicon Carbide Oxidation Growth Rates for Three-Dimensional Simulation, *Solid-State Electronics* (2016), doi: http://dx.doi.org/10.1016/j.sse.2016.10.032

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ACCEPTED MANUSCRIPT

Anisotropic Interpolation Method of Silicon Carbide Oxidation Growth Rates for Three-Dimensional Simulation

Vito Šimonka^{a,b}, Georg Nawratil^c, Andreas Hössinger^d, Josef Weinbub^{a,b}, Siegfried Selberherr^t

^aChristian Doppler Laboratory for High Performance TCAD at the

^bInstitute for Microelectronics, TU Wien, Gußhausstr. 27-29/E360, 1040 Wien, Austria ^cInstitute of Discrete Mathematics and Geometry, TU Wien, Wiedner Hauptstraße 8-10, 1040 Wien, Austria

issuite of Discrete Mainematics and Geometry, 10 wier, weater Haupstrape 8-10, 1040 wier, Austr

^dSilvaco Europe Ltd., Compass Point, St Ives, Cambridge, PE27 5JL, United Kingdom

Abstract

We investigate anisotropical and geometrical aspects of hexagonal structures of Silicon Carbide and propose a direction dependent interpolation method for oxidation growth rates. We compute three-dimensional oxidation rates and perform one-, two-, and three-dimensional simulations for 4H- and 6H-Silicon Carbide thermal oxidation. The rates of oxidation are computed according to the four known growth rate values for the Si- (0001), a- (1120), m- (1100), and C-face (0001). The simulations are based on the proposed interpolation method together with available thermal oxidation models. We additionally analyze the temperature dependence of Silicon Carbide oxidation rates for different crystal faces using Arrhenius plots. The proposed interpolation method is an essential step towards highly accurate three-dimensional oxide growth simulations which help to better understand the anisotropic nature and oxidation mechanism of Silicon Carbide.

Keywords: Silicon Carbide, Oxidation, Growth Rates, Anisotropy, Interpolation

1. Introduction

Silicon Carbide (SiC) has excellent physical properties and has received significant attention in recent years as a Silicon (Si) replacement material for power device applications due to a high electrical breakdown voltage and a high thermal conductivity. Compared to Si, SiC has approximately a three times wider band gap, ten times larger electrical breakdown voltage, and three times higher thermal conductivity [1, 2, 3]. Taking advantages of these properties, the on-state resistance for unipolar devices such as metal-oxide-semiconductor field-effect-transistors (MOSFET) can be reduced by a factor of a few hundreds when replacing Si with SiC [4, 5]. Aside from the theoretical advantages in SiC devices, the need for numerical simulation based on accurate models is indispensable to further the success of modern power electronics.

Among the numerous polytypes of SiC, most popular for device applications are 3C-SiC, 4H-SiC, 6H-SiC, and 15R-SiC. These polytypes are characterized by the stacking sequence of the bi-atom layers of the

Email address: simonka@iue.tuwien.ac.at (Vito Šimonka)

SiC structure. Changing the stacking sequence has a profound effect on the electrical properties. See Fig. 1a for an atomic view of a 4H-SiC. In this work, we focus on 4H- and 6H-SiC as they have been recognized as the most promising polytypes and are currently commercially available for high power, high frequency, and high temperature applications [6, 7].

Thermally grown oxide layers (SiO_2) play a unique role in device fabrication, e.g., lateral structures in planar technology and passivation of device surfaces. Therefore, it is necessary to have a solid understanding of oxidation growth rates and the dependence on the crystallographic planes of SiC. Among the wide bandgap semiconductors, SiC is the only compound semiconductor which can be thermally oxidized in the form of SiO₂, similar to conventional Si substrate. This is seen as one of the most important technological properties of SiC and has motivated considerable effort in its development. The following reaction governs the oxidation of SiC [1]:

$$\operatorname{SiC} + \frac{3}{2}\operatorname{O}_2 \leftrightarrow \operatorname{SiO}_2 + \operatorname{CO}.$$
 (1)

As opposed to the relatively simple oxidation of Si, the thermal oxidation of SiC includes five steps [2] (dis-

Preprint submitted to Solid-State Electronics

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