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Tuning the tunneling probability by mechanical stress in Schottky barrier based reconfigurable nanowire transistors

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ABSTRACT

Mechanical stress is an established and important tool of the semiconductor industry to improve the performance of modern transistors. It is well understood for the enhancement of carrier mobility but rather unexplored for the control of the tunneling probability for injection dominated research devices based on tunneling phenomena, such as tunnel FETs, resonant tunnel FETs and reconfigurable Schottky FETs. In this work, the effect of stress on the tunneling probability and overall transistor characteristics is studied by three-dimensional device simulations in the example of reconfigurable silicon nanowire Schottky barrier transistors using two independently gated Schottky junctions. To this end, four different stress sources are investigated. The effects of mechanical stress on the average effective tunneling mass and on the multi-valley band structure applying the deformation potential theory are being considered. The transfer characteristics of strained transistors in n- and p-configuration and corresponding charge carrier tunneling are analyzed with respect to the current ratio between electron and hole conduction. For the implementation of these devices into complementary circuits, the mandatory current ratio of unity can be achieved by appropriate mechanical stress either by nanowire oxidation or the application of a stressed top layer.

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1. Introduction

Reconfigurable nanowire (NW) transistors (RFETs) provide an increased functionality of highly integrated circuits beyond classical device scaling [1–3]. With its two independently gated Si-$NiSi_2$ Schottky junctions (SJ) at source and drain side the RFET is able to work as either a n-FET or a p-FET device using the same physical structure as defined by a programming voltage [4] (Fig. 1). The flexible programming feature at runtime enables the synthesis of logic circuits and gates with lower transistor count and reduced critical paths compared to CMOS based circuits. For example a logic gate cell containing only six RFETs can be switched between full-swing complementary NAND and NOR functionality even giving an equal delay for both functions [5]. Compact XOR functions in a transmission gate configuration have been proposed [6] and demonstrated [7] recently with only four RFETs. The same cell with a different wiring serves as a 3 input majority (MAJ) gate. Since arithmetic operations can be realized efficiently with XOR and MAJ gates novel opportunities for circuit design and design automation arise [6]. One-bit adders with half of the device count compared to CMOS could be shown recently [8]. Nevertheless, the drain currents of unstrained n- and p-RFETs with Si-$NiSi_2$ junctions (barrier for electrons ~0.66 eV, for holes ~0.46 eV) are not per-se symmetric and thus do not satisfy the requirements for complementary circuit operation using a device with identical geometry as n- and p-type transistor. Work-function/ band-offset tuning at the metal contacts or through doping is a difficult task in terms of variability at the nanometer-scale. In this work we employ mechanical stress to modify the band structure of the semiconductor nanowire channel yielding an effective mechanism to precisely adjust the symmetry between n- and p-RFET without the need of doping or altering the electrode material composition [9]. Process and device simulations were carried out with Sentaurus from Synopsys (K-2015.06) to analyze the NW induced stress profiles and the resulting transfer characteristics of n- and p-programmed RFETs [10]. Effective masses are determined by band structure

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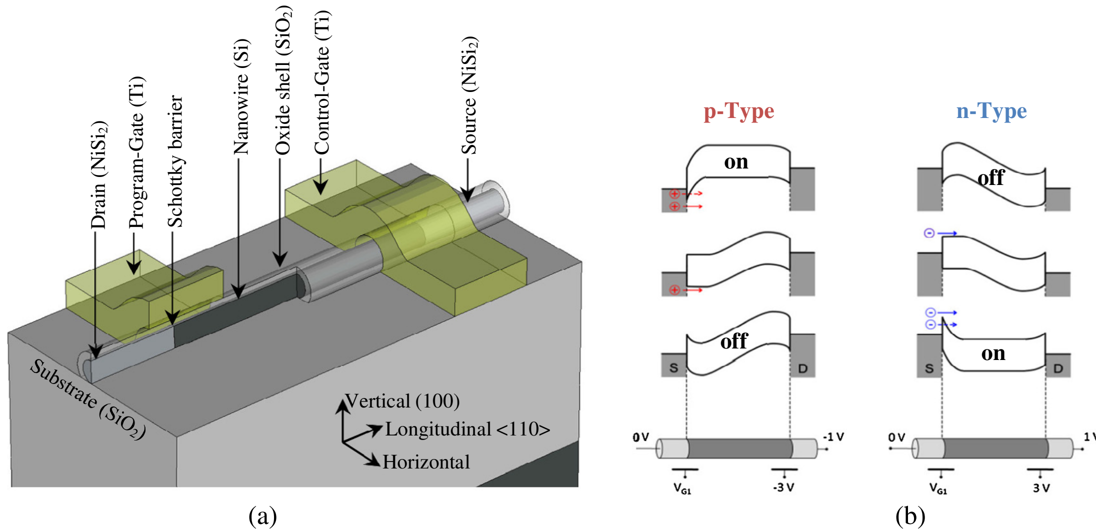

Fig. 1. Schematic view of a reconfigurable silicon NW-RFET with two independently gated Schottky junctions at source and drain, (a) RFET structure (b) operation states.

calculations based on the empirical pseudopotential method [11]. The induced mechanical stress was introduced by four different approaches as illustrated in Fig. 2. First, the self-limiting oxidation represents a reliable and uncomplicated way to form strong radial compressive stress and will be described in detail. Moreover, the simulated results could be verified by experimental data [12]. Nevertheless, a high gate oxide thickness can be detrimental to device performance, thus additional stressor vehicles are investigated: epitaxial stress from the silicidation of source/drain contacts, use of metal gate contacts with an intrinsic compressive stress and finally a tensile stressed top layer deposited on top of a geometrically optimized device.

The achieved results can also be applied to other type of devices encompassing tunneling through a barrier in the on-state, such as any Schottky FETs and in certain transport mechanisms of resonant tunneling transistors [13].

2. Mechanical stress of oxidized silicon NW

In the process simulation a 220 nm long and nearly 20 nm thick undoped silicon NW with a ⟨1 1 0⟩ channel direction and six facets (two times (1 0 0), four times (1 1 1)) was oxidized at 875 °C with 10 slm O_2 capturing the experimental structure reported in Ref. [12]. Note that the oxide reaction rate for (1 1 1) surfaces are 30–100% higher than for (1 0 0) resulting in an oval NW cross section. The appearing oxide has approximately twice the thickness versus the consumed silicon leading to a strong volume expansion of the silicon oxide shell and consequently giving a radial compressive stress in the silicon NW (Fig. 3). In addition, the stress modulated reaction rate at the Si-SiO_2 interfaces and the stress dependent oxygen diffusion in the tensile oxide shell cause a self-limitation of oxidation shown by the slightly saturating gate oxide thickness with increasing time in accordance with [14]. Both stress effects as

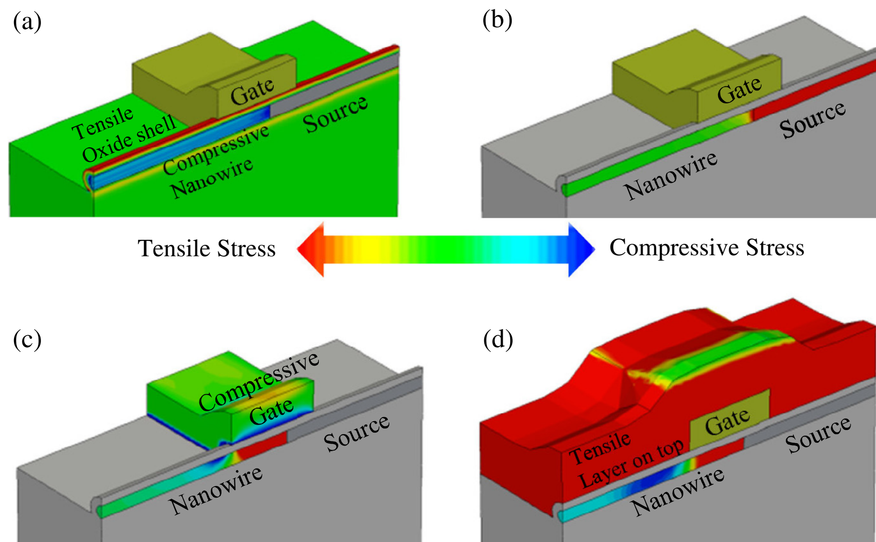

Fig. 2. Simulated stress profiles of silicon nanowire junctions induced by several stress sources: (a) compressive stress from oxide shell, (b) tensile stress from the silicidation of source/drain contacts, (c) compressively stressed metal gates and (d) tensile stressed layer on top of the device. (Stress scale is normalized to the maximum value for each case individually).

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