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Influence of the morphology of the copper(II) phthalocyanine thin film on the performance of organic field-effect transistors

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ABSTRACT

Organic thin-film transistors (OTFTs) with high crystallization copper phthalocyanine (CuPc) active layers were fabricated. The performance of CuPc OTFTs was studied without and with treatment by Solvent Vapor Annealing on CuPc film. The values of the threshold voltage without and with solvent-vapor annealing are −17 V and −10.5 V respectively. The field-effect mobility values in saturation region of CuPc thin-film transistors without and with Solvent Vapor Annealing are 0.00027 $cm^2/V\,s$ and 0.0025 $cm^2/V\,s$ respectively. Meanwhile, the high crystallization of the CuPc film with a larger grain size and less grain boundaries can be observed by investigating the morphology of the CuPc active layer through scanning electron microscopy and X-ray diffraction. The experimental results showed the decreased of the resistance of the conducting channel, that led to a performance improvement of the OTFTs.

1. Introduction

Organic thin-film transistors (OTFTs) have attracted a great deal of attention and experienced rapid development for a wide variety of applications, such as flexible displays, gas sensors, electronic paper, electronic bar codes, integrated circuits, etc. [1,2]. There are a large number of factors that affect the device performance. For instance, the choice of metal electrodes [3], dielectric material [4], organic semiconductor/metal interfaces and organic semiconductor/dielectric interfaces [5], the device configuration, organic semiconductor (conjugated polymers and small conjugated molecules with low molecular weight). Considering all of the above discussion, the choice of the organic semiconductor material will mainly determine the device performance. OTFTs show a strong relationship between the morphological structure of the material and the function of the device [6–8]. The film morphology will strongly influence the charge transport. The importance of the molecular ordering for fabricating OFETs with high performance is even more important in small-molecule-based transistors [9,10]. There are many kinds of methods of changing film morphology. such as substrate materials [10], deposition temperatures [10], Solution-based deposition methods(spin-coating [11] zone-casting [12], dip-coating [13,14], solution-sheareddeposition [15]) Postdeposition Treatments (Temperature annealing [16], solvent-assisted reannealing [17]), Single-Crystal [18,6].

Molecular selfassembled monolayers (SAMs) on the metal electrodes and on the dielectric have been proved to be a useful tool to control the molecular order [19]. It has been demonstrated that solvent-vapor annealing (SVA) is an effective way to improve device performance [20–25].

Copper phthalocyanine (CuPc) is a typical organic semiconductor material and a cheap, commercially available pigment that not only has high thermal and chemical stability, but also exhibits excellent field-effect properties [26,27]. Some studies have indicated that the morphology of the CuPc film depends on the substrate, heat-treatment temperatures, and condition of substrates during film deposition [10].

In this paper, using a typical organic semiconductor material, copper phthalocyanine (CuPc), we present an experimental study of influence of petroleum ether SVA on electrical characteristics and films surface morphologies of CuPc OTFTs with SiO_2 gate dielectric. The performance of CuPc thin-film transistors was studied without and with petroleum ether(PE) solvent-vapor annealing on CuPc layer. Electrical parameters as the threshold voltage, the

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field-effect mobility and the on-off current ratio have been estimated. Relationship of the quality of the electrical performance and crystalline morphology of the organic layer on CuPc OTFTs without and with treatment of petroleum ether SVA was investigated.

2. Experimental section

Heavily doped silicon wafers (0.013 Ω cm) were used as substrate and gate electrode. A 300 nm layer of SiO_2 was grown on top of silicon wafers by thermal oxidation and acted as a gate dielectric. The wafers were ultrasonically cleaned with acetone, isopropyl alcohol, and ultra purified water, successively. Then all wafers were inserted into octadecyltrichlorosilane (OTS) solution (methylbenzene as solvent)for 2 h to optimize surface properties. The SiO_2/OTS wafer has an apacitance of 8 nF/cm^2 measured by an Agilent E4980A LCR meter. CuPc was deposited by vacuum sublimation at an apparent fixed rate of 0.2 nm/s recorded by a quartz crystal oscillator at room temperatures under a background pressure of 7×10^{-4} Pa. CuPc was purchased from Aladdin Chemical Company without purification before use. The sublimation temperatures of the CuPc are 270 °C. The thicknesses of CuPc were carefully held at a constant at 40 nm. Subsequently, the samples were transferred into a jar filled with PE solvent, where it stayed for 4 h. After solvent annealing, the samples were dried overnight (>24 h) at room temperature. Finally, a 80 nm Cu film acting as source/drain electrodes was deposited by thermal evaporation through a shadow mask defining channel width (W) and length (L) of 1000 and 10 μm, respectively. Cu was deposited by vacuum sublimation at an apparent fixed rate of 0.2 nm/s recorded by a quartz crystal oscillator at room temperatures under a background pressure of 7×10^{-4} Pa. The thickness of Cu was recorded by a quartz crystal oscillator installed in the vacuum chamber. bottom-gate and bottom-contact configuration based on CuPc as active layer were fabricated in Fig. 1. The CuPc thin films have been characterized by X-ray diffraction (XRD), field emission scanning electron microscopy (FESEM). The XRD profiles were taken by using Rigaku D/max-2500 X-ray diffractometer with CuKa radiation (l¼ 1.5418 Å). FESEM (Model: Hitachi S-4800II型, Japan) was used to record the images of the CuPc thin films. The device performance was evaluated in air at room temperature by a Keithley 2400 Source Meter semiconductor analyzer.

3. Results and discussion

3.1. Film morphology characterization

The morphology of the CuPc film was studied by SEM and XRD. Fig. 2 shows the SEM images of CuPc films grown on SiO_2 gate dielectric without and with petroleum ether SVA. It can be seen that the film before SVA shows a worm-shaped grain with 50 nm wide and 100 nm long in Fig. 2a. In contrast, the image of CuPc thin film after petroleum ether SVA for 4 h is shown in Fig. 2b, which shows clearly the dense and uniform packing of nanoribbons with length ranging from 400 to 700 nm and width nearly 50 nm.

Fig. 3 shows the XRD images of CuPc films grown on SiO_2 gate dielectric without and with petroleum ether SVA. The diffraction peaks in the CuPc thin films grown on SiO_2 is weaker than that of the CuPc thin film after petroleum ether SVA grown on SiO_2. Such result demonstrates that the polycrystalline structure of CuPc is more intense in device with petroleum ether SVA. Therefore, the high crystallization of the CuPc film in device with petroleum ether SVA could lead to a higher electrical characteristic than that of the device without petroleum ether SVA.

3.2. Device characterization

A plot is shown in Fig. 4 which is the drain current (I_{ds}) versus the drain-source voltage (V_{ds}) for different gate-source voltages (V_{gs}) of the CuPc OTFT before SVA. That the increased of $-I_{ds}$ for the device with the increasing of $-V_{gs}$ implied characteristics of p-type. In Fig. 4, it is noted that the $-I_{ds}$ smoothly increased (i.e., ohmic behavior) with applying $-V_{ds}$ in the lower bias region for the device. It is also observed that the I_{ds} of the device were perfectly saturated as the V_{ds} in the higher bias region.

The hole mobility in the saturation region was calculated by Eq. (1):

$$I_{ds} = \frac{W}{2L} \cdot \mu C_i (V_{gs} - V_T)^2 \quad (1)$$

where W is the channel width, L is the channel length, C_i is the capacitance per unit area of the insulating layer. V_T is the threshold voltage, and u is the field-effect mobility, respectively. u can be calculated from the slope of the plot of $\sqrt{/I_{ds}/}$ versus V_{gs} for $V_{ds} = -20$ V (transfer characteristics) of the device, as shown in Fig. 5 which corresponds to Fig. 4. The mobility calculated in the saturation region is 0.00027 cm^2/V s at $V_{ds} = -30$ V, and the value of the threshold voltage is −17 V. The on–off current ratio estimated to be around 10.

Fig. 6 shows the output characteristics of the CuPc OTFT after petroleum ether SVA for 4 h, i.e., I_{ds} as a function of V_{ds} for different V_{gs}, can be seen. The device also exhibits the operating characteristics of a p-channel field-effect transistor, and saturation characteristics under higher negatively gate voltage. The $\sqrt{/I_{ds}/}$ versus V_{gs} curve in the saturation region for $V_{ds} = -30$ V is shown in Fig. 7. The values of the field-effect mobility, the threshold voltage and the on–off current ratio in the saturation region at Vds = −30 V are 0.0025 cm^2/V s, −10.5 V and 10^2–10^3 respectively.

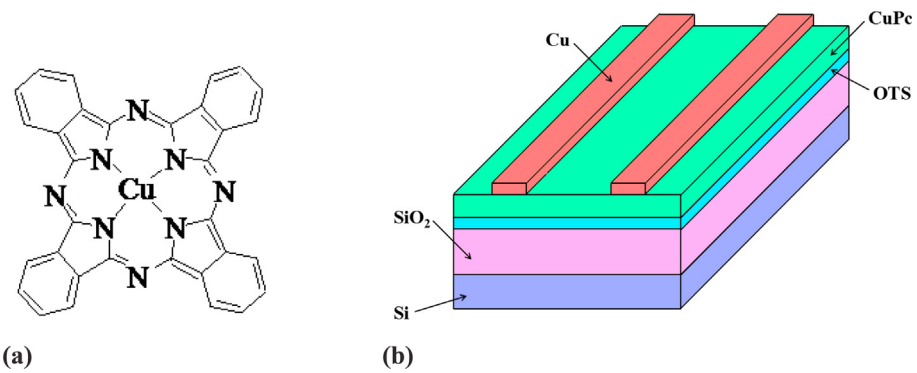

Fig. 1. (a) Chemical structure of CuPc. (b) The device configuration of organic thin-film transistors used in this work.