Solid-State Electronics 129 (2017) 6–9

Contents lists available at ScienceDirect

Solid-State Electronics

journal homepage: www.elsevier.com/locate/sse

Bottom-gate poly-Si thin-film transistors by nickel silicide seed-induced lateral crystallization with self-aligned lightly doped layer

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ARTICLE INFO

Article history:
Received 20 May 2016
Received in revised form 6 October 2016
Accepted 27 November 2016
Available online 5 December 2016

The review of this paper was arranged by Dr. Y. Kuk

Keywords:
Bottom-gate
Polycrystalline silicon (poly-Si)
Thin-film transistor (TFT)
Self-aligned
Hot-carrier
Kink-effect

ABSTRACT

We report a novel method to reduce source and drain (S/D) resistances, and to form a lightly doped layer (LDL) of bottom-gate polycrystalline silicon (poly-Si) thin-film transistors (TFTs). For application in driving TFTs, which operate under high drain voltage condition, poly-Si TFTs are needed in order to attain reliability against hot-carriers as well as high field-effect mobility (μ_{FE}). With an additional doping on the p^+ Si layer, sheet resistance on S/D was reduced by 37.5% and an LDL was introduced between the channel and drain. These results contributed to not only a lower leakage current and gate-induced drain leakage, but also high immunity of kink-effect and hot-carrier stress. Furthermore, the measured electrical characteristics exhibited a steep subthreshold slope of 190 mV/dec and high μ_{FE} of 263 cm^2/Vs.

1. Introduction

Among the various types of thin-film transistors (TFTs) (i.e., amorphous Si (a-Si), amorphous oxide semiconductor, and organic TFTs), the low temperature polycrystalline silicon (LTPS) TFT is the most promising candidate for application in active-matrix organic light-emitting diode (AMOLED) displays due to its high driving current and field-effect mobility (μ_{FE}) [1,2,14]. Therefore, LTPS TFTs can increase the response speed of pixels and are suitable for application in a system-on-panel (SOP) since it can be integrated with a peripheral circuit directly on glass substrates [3]. However, to integrate the peripheral circuits on the same glass substrate, it is necessary to have not only a large driving current maintaining low leakage current, but also stable operation with high immunity of hot-carrier stress (HCS) [4–6,9]. For low leakage current and stable operation, polycrystalline silicon (poly-Si) TFTs with a lightly doped drain (LDD), offset gate, and gate-overlapped LDD structures have been proposed and demonstrated [7,8]. Although these structures effectively reduce leakage current and can obtain better drain field relief, they inevitably decrease the on-state current due to increased series resistance or channel length [8]. To overcome these problems, a raised source/drain (RSD) has been proposed. The RSD has the advantage of reduction of the source and drain (S/D), the series, and the contact resistances, as well as the lateral electric field, resulting in stable operation against HCS [8,9]. However, the RSD with a top-gate structure requires additional masks to achieve general channel thickness because the channel and S/D are deposited on the same layer; therefore, the entire process becomes complicated.

In this paper, we fabricated bottom-gate poly-Si (BGPS) TFTs by nickel silicide-induced lateral crystallization (SILC) (hereinafter "SILC-BGPS TFT") with a lightly doped layer (LDL). Also, we investigated the effect of additional doping on various thicknesses of p^+ Si layer. The electrical characteristics of the SILC-BGPS TFTs with an additional doping were also investigated.

2. Experiment

The conventional SILC-BGPS TFT (hereinafter "Conv-TFT") was fabricated for comparison [10,15]. First, a 300-nm-thick MoW as a gate electrode was deposited on a glass substrate with a 100-nm-thick SiO_x as a buffer layer and patterned. An 80-nm-thick SiN_x as a gate insulator, a 50-nm-thick a-Si as an active layer, and a 100-nm-thick SiO_x as an etch stopper (E/S) were successively deposited by plasma-enhanced chemical vapor deposition (PECVD) at 350 °C. The E/S was patterned and etched in buffered oxide etchant (BOE) and then a p^+ Si was deposited by PECVD at 350 °C. To confirm the

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http://dx.doi.org/10.1016/j.sse.2016.11.019
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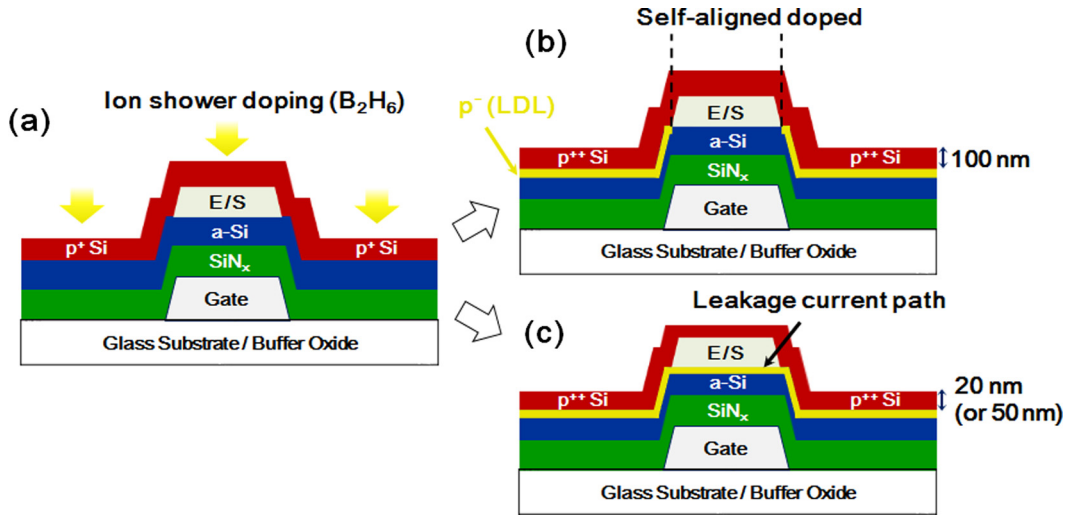

Fig. 1. Schematic diagrams of LDL-TFTs (a) before and (b), (c) after doping. The thicknesses of p^+ Si are (b) 100 nm and (c) 20 nm or 50 nm.

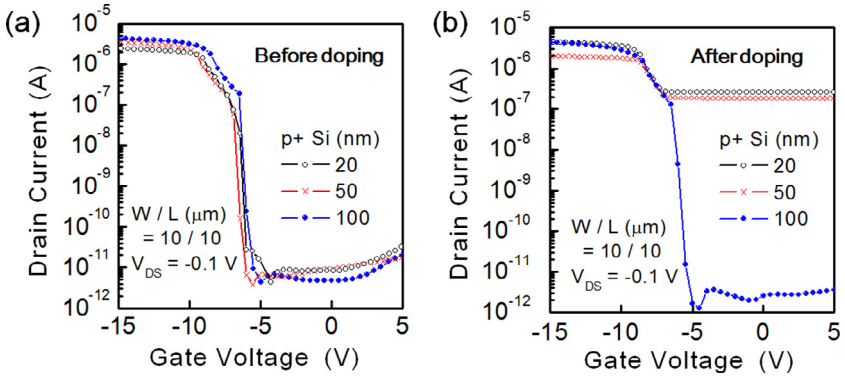

Fig. 2. The transfer characteristics of S1LC-BGPS TFTs with various thicknesses of p^+ Si (a) without and (b) with an additional doping on the p^+ Si surface.

effect of the additional doping, three samples were fabricated with various thicknesses of the p^+ Si (20 nm, 50 nm, and 100 nm). Compared with the Conv-TFT, other samples implemented an ion shower doping using B_2H_6 on the entire p^+ Si layer with 17 kV of accelerated voltage and 150 W of radio-frequency power for 10 min as shown in Fig. 1(a). Then, the p^+ Si, a-Si, and gate insulator were etched by reactive ion etching (RIE) without breaking the vacuum. Afterward, the Ni pattern was defined and 5-nm-thick Ni was sputtered on the S/D. The Ni was removed in H_2SO_4 for SILC; then, Ni silicides remained on the S/D and the Ni pattern was removed using a lift-off method [10]. The samples were annealed in a furnace at 570 °C in a vacuum for 2 h for crystallization followed with H_2 ambient for 1 h H_2 passivation. Finally, passivation with a 300-nm-thick SiO_x and metallization with a 500-nm-thick MoW were implemented. After completing the entire process, the electrical characteristics were measured with Keithley 2636 and Agilent E5270B systems. All of the fabrication processes were carried out in a 1000-class clean room.

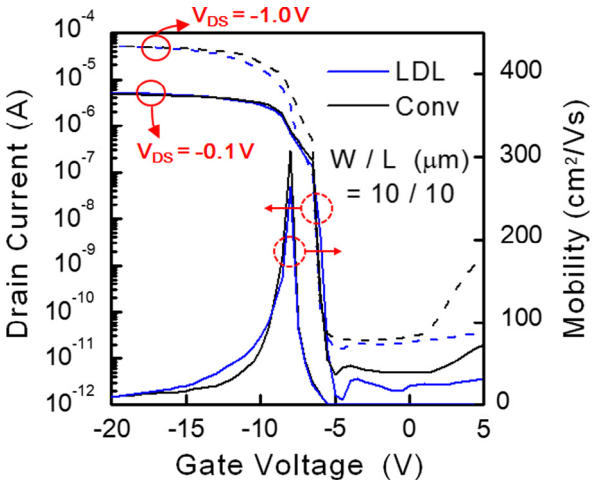

Fig. 3. The transfer characteristics of the LDL- and Conv-TFTs, which were extracted from the p^+ 100 nm graphs of Fig. 2.

3. Results and discussion

The transfer characteristics of the SILC-BGPS TFTs with various thicknesses of the p^+ Si are presented in Fig. 2. Unlike that shown in Fig. 2(a), an additional doping on the p^+ Si surface was implemented as shown in Fig. 2(b). For the p^+ Si thicknesses of 20 nm and 50 nm, the leakage current greatly increased by more than four orders of magnitude. It can be said that the upper surface of the channel was doped by boron penetrating both the p^+ Si and E/S layers under this doping condition, and the leakage current path was then generated immediately below the E/S after doping (Fig. 1(c)). For the on-state current, a significant variation did not manifest because the electrons were pushed toward the direction below