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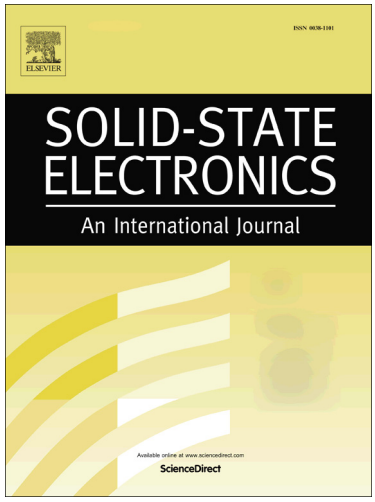

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ACCEPTED MANUSCRIPT

Two Methods of Tuning Threshold Voltage of Bulk FinFETs with Replacement High-k Metal-Gate Stacks

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Abstract

In this work, we propose two threshold voltage (V_{TH}) tuning methods for bulk FinFETs with replacement high-k metal gate. The first method is to perform a vertical implantation into fin structure after dummy gate removal, self-aligned forming halo & punch through stop pocket (halo & PTSP) doping profile. The second method is to execute P^+ / BF_2^+ ion implantations into the single common work function (WF) layer in N- / P-FinFETs, respectively. These two methods have been investigated by TCAD simulations and MOS-capacitor experiments respectively, and then integrated into FinFET fabrication successfully. Experimental results show that the halo & PTSP doping profile can reduce V_{TH} roll off and total variation. With P^+ / BF_2^+ doped WF layer, the $V_{TH\text{-}sat}$ shift -0.43 V / +1.26 V for N-FinFETs and -0.75 V / +0.11 V for P-FinFETs, respectively, with gate length of 500 nm. The proposed two methods are simple and effective for FinFET V_{TH} tuning, and have potential for future application of massive production.

Keywords

FinFET, Halo, Work Function, Punch Through Stop Pocket, Threshold Voltage, High k Metal Gate

1. Introduction

FinFET has emerged as a device structure to enable down scaling at and beyond the 22 nm technology node. Precise threshold voltage (V_{TH}) control and multiple V_{TH} levels are required for FinFET application.

V_{TH} of a FinFET is less sensitive to the channel implantation implemented after STI recessing and fin height definition, because of a dose-loss mechanism occurring in the narrow fins [1]. Therefore, proper halo design is allowed in FinFETs to improve Short Channel Effect (SCE) and reduce V_{TH} variation [2]. However, as CMOS dimensions continue to shrink, conventional angular halo implantations face challenges such as gate- or fin-shadowing effect [3], which are particularly troublesome for big aspect ratio in advanced CMOS technology [4].

To achieve different V_{TH} with low channel doping, gate work-function (WF) engineering with multiple metal layers [5,6] has been used, but the integration process is very complex. Implanting ions into a single gate/dielectric stack remains the simplest and most cost-effective method. Many studies have been reported [7-12]. Dipole formation models [13,14] for V_{TH} tuning are also formulated. By implanting P^+ / BF_2^+ into a single common WF layer, we have achieved dual band-edge effective WF for planar CMOS device [15] with the replacement high-k/metal gate (HKMG) process.

In this work, we propose two V_{TH} tuning methods with implantations for replacement HKMG FinFETs. The first method is to form a halo & punch through stop pocket (halo & PTSP) doping profile in fin structure using a single vertical implantation after dummy gate removal. The halo & PTSP doping profile can reduce V_{TH} variation. The second method is to introduce P^+ / BF_2^+ ions into FinFET metal gate WF layer. Using P^+ / BF_2^+ implantations, we have achieved three V_{TH} levels for FinFETs. The proposed two V_{TH} tuning techniques are simple, low-cost, and fully compatible with state-of-the-art FinFET process flow, and thus have potential for future application of massive production.

2. Proposed Methods

2.1. Self-aligned halo & PTSP

In a bulk FinFET, to suppress current leakage between source and drain (S/D) through bottom part of the fin (sub fin), punch-through stop layer (PTSL) is formed, which is a relatively high-concentration doping layer beneath the channel. One of the simplest methods to form PTSL is ion implantation.

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