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A High-Speed Lateral PIN Polysilicon Photodiode on Standard Bulk CMOS Process

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Abstract: This paper reports a lateral PIN polysilicon photodiode on standard bulk complementary metal-oxide-semiconductor (CMOS) process for monolithically integrated high-speed optoelectronic integrated circuits (OEIC). A nominal undoped polysilicon as the photodetection area is intentionally created without introducing any process modification. With the device area of $50 \times 50 \mu\text{m}^2$, a measured responsivity of 46mA/W and a quantum efficiency of 11% were observed under the reverse voltage of 10V and the wavelength of 520nm. A compact equivalent circuit model for the proposed lateral photodiode is built to analyze the frequency response, and a bandwidth of over 20GHz was obtained from the measured data, which is to the best of our knowledge the largest bandwidth ever reported based on standard bulk CMOS process.

Keywords: Polysilicon photodiode; high-speed optical interconnection; optoelectronic integrated circuits (OEIC); responsivity; bandwidth; standard bulk complementary metal-oxide-semiconductor (CMOS)

1. INTRODUCTION

Short distance high-speed optical communication, such as chip-to-chip and board-to-board interconnections, and single-chip optoelectronic integrated circuits (OEIC) are attracting increasing research interests. For an optical receiver, one of the most important devices is the photodetector. From cost and performance perspective, it's preferred to monolithically integrate the photodetector with the circuit using standard complementary metal-oxide-semiconductor (CMOS) process. The Silicon-on-Insulator (SOI) CMOS is able to provide much higher performance compared to the bulk CMOS because of its substrate isolation structure and lower parasitic capacitance. In [1], the SOI-based lateral PIN photodiode with the device area of $75 \times 75 \mu\text{m}^2$ can provide high bandwidth of over 10GHz. However, the bulk CMOS is much more popular than SOI CMOS because of its much lower cost. Various kinds of diodes available in bulk CMOS process were investigated, and many techniques were proposed to reduce the impact of slow diffusion current and improve the frequency response [2-6]. In [2], the nwell-substrate diode was used, and a meshed spatially-modulated scheme was proposed. A bandwidth of 6.9GHz and a responsivity of 29mA/W were achieved with the device area of $55 \times 55 \mu\text{m}^2$. In [3], the n^+ -pwell diode enclosed by deep-nwell was used, and a deep-nwell bias scheme was

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