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PII: S0038-1101(16)30383-5
DOI: http://dx.doi.org/10.1016/j.sse.2016.12.015
Reference: SSE 7173

To appear in: *Solid-State Electronics*

Received Date: 6 April 2016
Revised Date: 2 December 2016
Accepted Date: 26 December 2016

Please cite this article as: Al-Ameri, T., Georgiev, V.P., Sadi, T., Wang, Y., Adamu-Lema, F., Wang, X., Amoroso, S.M., Towie, E., Brown, A., Asenov, A., Impact of Quantum Confinement on Transport and the Electrostatic Driven Performance of Silicon Nanowire Transistors at the Scaling Limit, *Solid-State Electronics* (2016), doi: http://dx.doi.org/10.1016/j.sse.2016.12.015

Impact of Quantum Confinement on Transport and the Electrostatic Driven Performance of Silicon Nanowire Transistors at the Scaling Limit

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***Abstract*—In this work we investigate the impact of quantum mechanical effects on the device performance of n-type silicon nanowire transistors (NWT) for possible future CMOS applications at the scaling limit. For the purpose of this paper, we created Si NWTs with two channel crystallographic orientations <110> and <100> and six different cross-section profiles. In the first part, we study the impact of quantum corrections on the gate capacitance and mobile charge in the channel. The mobile charge to gate capacitance ratio, which is an indicator of the intrinsic performance of the NWTs, is also investigated. The influence of the rotating of the NWTs cross-sectional geometry by 90º on charge distribution in the channel is also studied. We compare the correlation between the charge profile in the channel and cross-sectional dimension for circular transistor with four different cross-sections diameters: 5nm, 6nm, 7nm and 8nm. In the second part of this paper, we expand the computational study by including different gate lengths for some of the Si NWTs. As a result, we establish a correlation between the mobile charge distribution in the channel and the gate capacitance, drain-induced barrier lowering (DIBL) and the subthreshold slope (SS). All calculations are based on a quantum mechanical description of the mobile charge distribution in the channel. This description is based on the solution of the Schrödinger equation in NWT cross sections along the current path, which is mandatory for nanowires with such ultra-scale dimensions.**

***Index Terms*— CMOS, electrostatics, nanowire transistors, performance, quantum effects, TCAD.**

I. INTRODUCTION

The gate-all-around (GAA) silicon nanowire transistors (NWT) have the potential to extend Moore's law beyond the 7nm mark [1-3]. One of the major reasons being that the GAA design provides the best electrostatic integrity in comparison to all other transistors architectures and therefore the best gate control over the channel [4-7]. However, in such ultra-scaled GAA NWT, the quantum mechanical effects play a significant role and they must be considered in order to obtain accurate device performance results [8-10]. For example, the quantum confinement effects lead to quantum threshold voltage shifts, simultaneously reducing the gate-to-channel capacitance and the available charge for transport in the channel [11-13]. The reduced gate-to-channel capacitance also has a negative effect on the electrostatic integrity. The impact of the above effects increases with the reduction of the characteristic confined dimensions and therefore it will play a critical role in simulation-based research and design of NWT-based CMOS technology at the scaling limits.

Moreover, the improvement in electrostatics can lead to much shorter effective channel length which can increase the density of integration. Also, in conventional transistors minimising the interaction between the source and drain is critical for the improvement of the short-channel effects. The short channel-effects can be characterized by the drain-induced barrier lowering (DIBL), sub-threshold (SS) slope and the threshold voltage roll-off [14-16]. These effects create technical and scientific challenges, which can be tackled by a careful device design consideration [2, 17].

Overall, in this paper, taking into account the quantum confinement effects, we provide a comprehensive overview of the performance of numerous GAA NWTs as a function of cross-section shape and area, channel length, crystallographic orientation and different gate materials. The ultimate goal is to establish the strengths and weaknesses of such devices and determine the best design configuration and parameters for a specific application.

The next section describes the template transistors, where the methodology is revealed in Section III. The major results and analysis on the impact of quantum confinement on gate capacitance, charge and short channel effects are presented in Sections IV and V. Section V concludes the paper.

II. SIMULATED NANOWIRE TRANSISTOR

The simulated NWTs considered in this subsection of the paper have four different cross-sections: cylindrical, elliptical, square and rectangular, which are schematically presented in Fig. 1. The elliptical and rectangular NWTs have two different heights and widths of the wires but more importantly all devices have an identical cross-section area of 4π nm^2. The precise cross-sectional dimensions for all six wires are shown in Table 1. Two channel crystallographic orientations on (001) wafer are considered: <110> and <100>. Table 2 reveals the