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Extraction method for parasitic capacitances and inductances of HEMT models

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ABSTRACT

A new method to extract parasitic capacitances and inductances for high electron-mobility transistors (HEMTs) is proposed in this paper. Compared with the conventional extraction method, the depletion layer is modeled as a physically significant capacitance model and the extrinsic values obtained are much closer to the actual results. In order to simulate the high frequency behaviour with higher precision, series parasitic inductances are introduced into the cold pinch-off model which is used to extract capacitances at low frequency and the reactive elements can be determined simultaneously over the measured frequency range. The values obtained by this method can be used to establish a 16-elements small-signal equivalent circuit model under different bias conditions. The results show good agreements between the simulated and measured scattering parameters up to 30 GHz.

1. Introduction

With the rapid development of communication technology, gallium nitride (GaN)-based HEMTs become attractive candidates in microwave and millimeter-wave frequency applications because GaN transistors have the excellent performance in terms of power density, breakdown voltage and electron saturation velocity. The accurate small-signal model of FETs is very useful for the device performance analysis (gain, noise, etc.) and it can be also used for the large-signal nonlinear model construction [1,2]. The fast and rigorous method of parameter extraction plays a crucial role in the establishment of the models. Direct extraction method [3–6] and the optimization technique [7,8] are based on two common extraction methods for small-signal equivalent circuits.

The open test structure method [9,10] and the pinch-off cold-FET method have been proposed to extract parasitic capacitances. The first method requires a specific test structure and the accuracy of this technique is high. Gao et al. [11] proposed a direct extraction method for extrinsic capacitances of PHEMTs, which was based on a scalable small-signal model under pinch-off condition, the voltage of the gate was set under the threshold voltage and the drain-to-source bias was set to zero. In Ref. [3], two identical capacitors C_b were used to model the gate-to-source and gate-to-drain depletion layer capacitances. Lack of the drain-to-source capacitance will lead to the overestimation of the C_{pd} and the inaccurate C_{pd} will cause errors in the intrinsic parameter extraction. White et al. [4] added the third capacitance which was equal to C_b on the basis of the Dambrine's method. The drain-to-source capacitance should be smaller than the other intrinsic capacitances so the C_{pd} obtained by this method was questionable. In Lai's method [12], two identical capacitances C_b were used to describe the depletion layer extension under the gate and a capacitance C_c was introduced to account for drain-to-source capacitance. All conventional cold-FET methods are based on the source-drain symmetric structure and a common assumption that the C_{gs} is equal to C_{gd}.

Conventionally, the parasitic capacitances are determined from the measured Y-parameters of the total equivalent circuit under the pinched-off cold-FET condition at the low frequency and the relationship between the imaginary part of the Y-parameters and the capacitances is linear with the angular frequency [3–6]. But at the high frequency, there is a deviation from this linear relation after subtracting the influence of the extrinsic inductances [12]. In the conventional simplified equivalent circuit for capacitance extraction, the extrinsic inductances were not taken into account. However, inductances are included in the measured Y-parameters which are used to determine the parasitic capacitances. Therefore, the accuracy of the capacitance values is questionable.

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In this paper, a novel extraction method for parasitic capacitances and inductances is proposed to solve the problems of conventional approaches. In contrast with previous researches [3–6], the proposed method in this paper has high precision and no complex extraction procedure. In order to reduce the errors particularly at the high frequency when extracting the parasitic capacitances, series inductors are added into the reduced pinch-off cold-FET equivalent circuit. The capacitors and inductors can be determined simultaneously over the measured frequency range. Then, there are no limitations and assumptions at all on the depletion layer capacitances under pinch-off bias condition. The depletion layer extension is described into three capacitors. Eventually, the high precision of the values obtained by the proposed method have been validated by the open-short test structure method.

This paper is organized as follows. Section 2 introduces the structure of the measured device and the small-signal equivalent circuit model. The extracted procedure is described in detail in Section 3. Section 4 presents some comparisons and discussion. The experimental results and conclusions are shown in Sections 5 and 6, respectively.

2. Device structure and the model description

Fig. 1 shows the cross section and photograph of the measured device with a gate length of 0.4 μm and a gate width of 10 × 125 μm. The detailed technological process is described in [13].

Fig. 2 shows the small-signal electrical equivalent circuit topology for this device. The equivalent circuit can be categorized into extrinsic part and intrinsic part. L_g, L_s and L_d represent the gate, source and drain electrode inductances; R_s and R_d are the source and drain resistances, and R_g is the gate distributed resistance; C_{pg} and C_{pd} are the gate and drain pad extrinsic capacitances; C_{gs}, C_{gd} and C_{ds} represent the gate-source, gate-drain, and drain-source capacitances, respectively; R_i, R_{gd} and R_{ds} are the charge and output resistances; t and g_m are the intrinsic delay and intrinsic transconductance, correspondingly. C_{gs}, C_{gd}, C_{ds}, R_i, R_{gd}, R_{ds}, t and g_m are intrinsic elements which are emphasized by the dashed frame in Fig. 2. The rest are extrinsic elements which are assumed to be bias independent.

3. Extraction procedure

The simplified equivalent circuit in the dashed box of Fig. 3 is used to extract the parasitic capacitances at the low frequency by

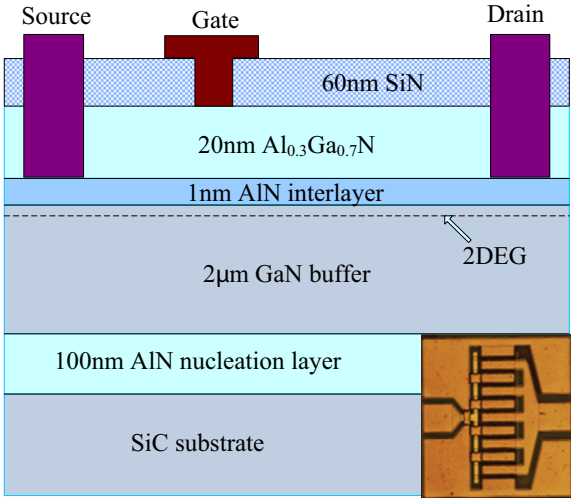

Fig. 1. The structure and photograph of the AlGaN/GaN HEMT.

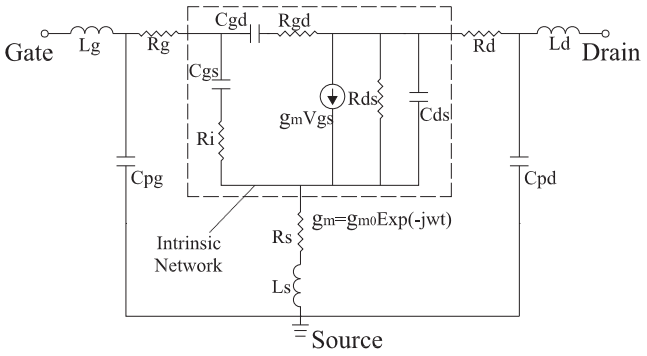

Fig. 2. Small-signal equivalent circuit for the HEMTs.

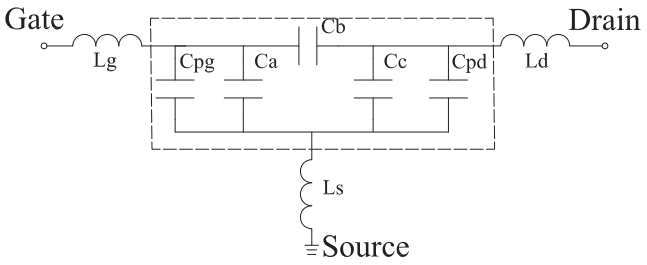

Fig. 3. Model for parameter extraction in this study.

many researchers [3,4,6,11]. At $V_{gs} < -V_{th}$ and zero drain current in the channel, the drain current source and the output channel conductance can be excluded. In this work, the series inductances are introduced into the conventional reduced equivalent circuit and the model for parameter extraction is shown in Fig. 3, where C_a, C_b and C_c represent the depletion layer capacitors. Because the parasitic resistances have no effect on imaginary parts of Z-parameters, the effect of resistances can be ignored during the extraction for parasitic capacitances and inductances.

The dashed box part in Fig. 3 can be expressed by the following Y-parameter matrix:

$$[Y] = \begin{pmatrix} j\omega(C_{gso} + C_b) & -j\omega C_b \\ -j\omega C_b & j\omega(C_{dso} + C_b) \end{pmatrix} \tag{1}$$

where

$$C_{gso} = C_{pg} + C_a \tag{2}$$

$$C_{dso} = C_{pd} + C_c \tag{3}$$

The Y-parameter matrix can be transformed into the Z-parameter matrix.

$$[Z] = [Y]^{-1} = \begin{pmatrix} \frac{M+(C_b)^2}{j\omega M(C_{gso}+C_b)} & \frac{C_b}{j\omega M} \\ \frac{C_b}{j\omega M} & \frac{C_{gso}+C_b}{j\omega M} \end{pmatrix} \tag{4}$$

where

$$M = C_{gso} \times C_{dso} + C_b \times C_{gso} + C_b \times C_{dso} \tag{5}$$

With addition of the parasitic inductances L_g, L_s and L_d, the Z-parameter of Fig. 3 (Z_L) can be obtained. We have

$$Z_{L11} = j\omega(L_g + L_s) + \frac{M + (C_b)^2}{j\omega M(C_{gso} + C_b)} \tag{6}$$

$$Z_{L12} = Z_{L21} = j\omega L_s + \frac{C_b}{j\omega M} \tag{7}$$

$$Z_{L22} = j\omega(L_d + L_s) + \frac{C_{gso} + C_b}{j\omega M} \tag{8}$$