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An ultra-wideband CMOS PA with dummy filling for reliability

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ABSTRACT

A V-band power amplifier in a bulk 65 nm CMOS technology with a peak gain 14.5 dB and 3-dB bandwidth of 28.8 GHz (50.8–79.6 GHz) is presented. The techniques to boost bandwidth and power efficiency are presented. In addition, the design of dummy filling to satisfy manufacturing density requirements while having negligible effects on performances is discussed in details. The PA features a three stage transformer coupled differential architecture with integrated input and output baluns on-chip. The PA achieves a measured saturated output power of 15.1 dBm and output 1 dB compression power of 12.9 dBm at 65 GHz. The peak power-added efficiency is 18.9%. The entire PA occupies area of 0.31 mm^2, while consuming 150 mW from a 1.25 V supply.

1. Introduction

The unlicensed multi-gigahertz bandwidth around 60 GHz is a good candidate for high data rate, short-range, and point-to-point wireless communication systems. CMOS technologies are attractive for the advantages of low power consumption, low cost, and high level integration with baseband. A CMOS-based 60 GHz power amplifier remains a challenge mainly due to low output power and low power added efficiency (PAE). Power combining techniques are typically used to achieve higher output power, albeit at the cost of reduced efficiency. For the high speed and wide bandwidth data communication applications, the PA is required to broaden the operation bandwidth. The main challenge of designing a PA over a broadband frequency range is to simultaneously match the optimum load impedance and maintain broadband gain performance. Distributed amplifiers are well-known approaches for wideband application, but large power dissipation degrades power efficiency. Also, distributed amplifiers usually occupy large chip area. A large number of 60 GHz PAs have been reported [1–11] over the past decade. However, trade-offs are still challenging between key specifications, such as gain, power efficiency, and bandwidth. Therefore, techniques to boost power amplifier bandwidth while maintaining high output power and high efficiency are desired.

CMOS technologies' rapid advancements over the past decade support increasing circuit speed, resulting in the wide adoption of mm-wave CMOS circuits today. However, the CMOS mm-wave power amplifiers are still challenging. First, although intrinsic CMOS device speed keeps increasing, the shrinking power supply voltages challenge high power delivery. Second, lossy substrates and high contact resistance degrade the quality factor of passive components and decrease power efficiency. Third, a larger portion of parasitic capacitance versus intrinsic capacitance erodes achievable operating frequency and further wastes power through the additional charging/discharging current to the parasitics. In addition, the main drive for CMOS technologies for integration with analog and digital sub-systems for SOC, on the other hand, imposes large coupling and interference among circuit blocks. Moreover, deep-scaled technologies have very tight design rule check (DRC) requirements, including local and global density requirements to ensure reliability. These requirements therefore impose a significant challenge to high frequency design with the need of passive components, such as inductors and transformers. To overcome these challenges in deep-scaled CMOS technologies, we adopted a transformer-based output matching network. The matching network transforms the 50 Ω output load impedance to the optimum load impedance over a broadband frequency to achieve high output power and PAE. The offset frequency tuning scheme and transformer based inter-stage matching network were used to obtain broadband gain performance. Moreover, well-designed metal dummy filling is presented to increase PA reliability.

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This paper is organized as follows. Section 2 discusses the design details of the transformer coupled differential wideband PA to enhance the bandwidth and increase power efficiency. Section 3 presents the detailed theoretical analysis of dummy effects and provides design insight for dummy filling for high reliability while minimizing performance degradation. Section 4 presents measurement results, and is then followed by a conclusion in Section 5.

2. Wideband PA design

Fig. 1 presents the schematic of a transformer-coupled three-stage differential PA with integrated input and output baluns [15]. Transformer based inter-stage matching and tuning is adopted due to its advantages of compactness, differential configuration, and good isolation between input and output for better stability. Also, DC biasing is applied at the center tap of the transformer, so DC block capacitors, RF chokes, and bypass capacitors can be eliminated for a considerable space reduction. The input and output transformers serve as baluns to convert between single-ended I/O signals and differential on-chip signals. Each stage is a differential NMOS common-source amplifier to achieve larger headroom and higher linearity.

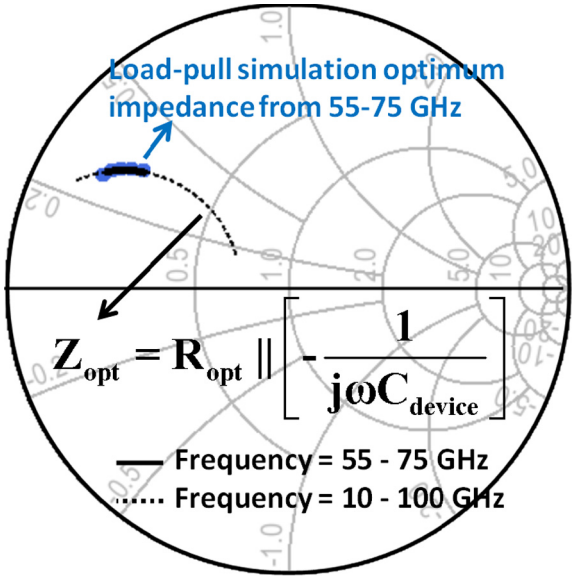

Fig. 2. Broadband optimum load impedance for a pair of differential pair transistor with the size of 89.44 μm/60 nm.

2.1. The wideband transformer-based output matching network

To achieve high output power and high efficiency over the entire frequency range, the output matching network should be designed to transform the load to the optimum impedance across the entire frequency range of interest. The optimum impedance is determined by performing large-signal load-pull simulation and it can be represented as [12]:

$$Z_{opt} = R_{opt} || X_{\text{opt}} \tag{1}$$

The parallel resistive portion R_{opt} is chosen for maximum peak PAE, and the device output capacitance C_{device} is tuned out by choosing

$$X_{\text{opt}} = -\frac{1}{j\omega C_{device}} \tag{2}$$

A large signal, load-pull simulation for maximum peak PAE is performed for a differential common-source amplifier with a transistor width of 89.44 μm from 55 GHz to 75 GHz. As shown in Fig. 2, the optimum impedance fits the Z_{opt} where $R_{\text{opt}} = 71.43\ \Omega$ and $C_{\text{device}} = 58.77$ fF. To achieve a broadband operation PA, we employed a transformer based matching network to transform the 50 Ω output load to the optimum impedance across the operation frequency range.

Fig. 3 shows the equivalent model of the output stage with a transformer based matching network [13]. The output device is modeled as a current source shunt with a parallel RC network. Here, C_{device} represents the drain capacitance of the transistor, and R_{opt} is determined through large signal load-pull simulation. The output matching network is composed of a transformer and a shunt capacitor C_2, which comes from the output pad and the transformer parasitics. The transformer is modeled with two coupled inductors, L_1 and L_2, with coupling coefficient k. Here, R_{s1} and R_{s2} represent the parasitic resistances of the inductors L_1 and L_2, respectively. The mutual inductance M is:

$$M = k\sqrt{L_1 L_2} \tag{3}$$

To simplify the analysis, we make the self-resonant frequencies on the primary and secondary sides identical by setting:

$$\omega_0 = \frac{1}{\sqrt{L_1 C_{device}}} = \frac{1}{\sqrt{L_2 C_2}} \tag{4}$$

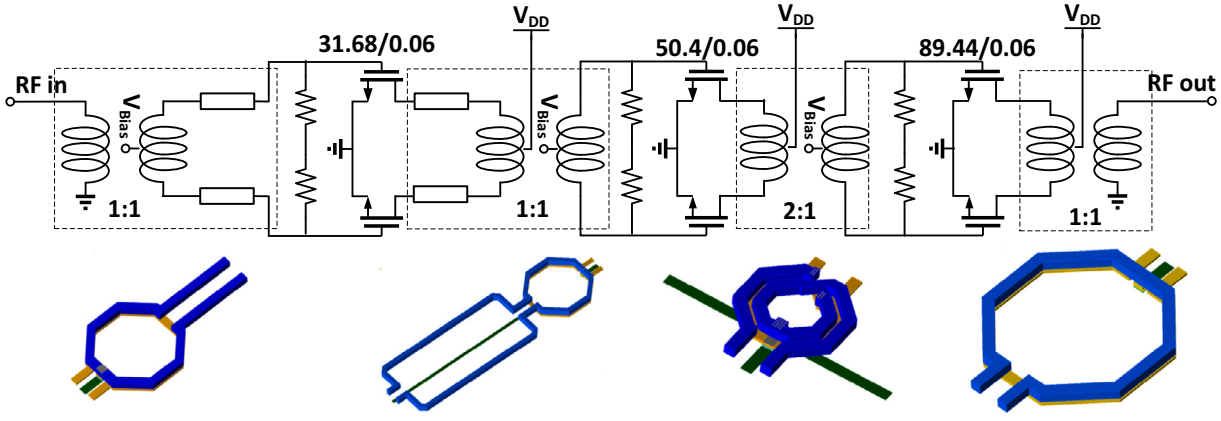

Fig. 1. Topology of the three-stage differential PA.

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