



Contents lists available at ScienceDirect

Solid-State Electronics

journal homepage: www.elsevier.com/locate/sse

Experimental study on the 4H-SiC-based VDMOSFETs with lightly doped P-well field-limiting rings termination

Yan Jing He^{a,b}, Hong Liang Lv^{a,b}, Xiao Yan Tang^{a,b,*}, Qing Wen Song^{b,c}, Yi Meng Zhang^{a,b}, Chao Han^{a,b}, Yi Men Zhang^{a,b}, Yu Ming Zhang^{a,b}

^a School of Microelectronics, Xidian University, Xi'an 710071, China

^b Key Laboratory of Wide Band Gap Semiconductor Technology, Xidian University, Xi'an 710071, China

^c School of Advanced Materials and Nanotechnology, Xidian University, Xi'an 710071, China

ARTICLE INFO

Article history:

Received 3 August 2016

Received in revised form 26 October 2016

Accepted 21 November 2016

Available online xxx

The review of this paper was arranged by Prof. S. Cristoloveanu

Keywords:

4H-SiC

VDMOSFET

Breakdown voltage

Junction termination

ABSTRACT

A lightly doped P-well field-limiting rings (FLRs) termination on 4H-SiC vertical double-implanted metal-oxide-semiconductor field-effect transistors (VDMOSFETs) has been investigated. Based on the simulation, the proposed termination applied to 4H-SiC VDMOSFET could achieve an almost same breakdown voltage (BV) and have the advantage of lower ion-implantation damage comparing with P⁺ FLRs termination. Meanwhile, this kind of termination also reduces the difficulty and consumption of fabrication process. 4H-SiC VDMOSFETs with lightly doped P-well (FLRs) termination have been fabricated on 10 μm thick epi-layer with nitrogen doping concentration of $6.2 \times 10^{15} \text{ cm}^{-3}$. The maximum breakdown voltage of the 4H-SiC VDMOSFETs has achieved as high as 1610 V at a current of 15 μA, which is very close to the simulated result of 1643 V and about 90% of the plane parallel breakdown voltage of 1780 V. It is considered that P-well FLRs termination is an effective, robust and process-tolerant termination structure suitable for 4H-SiC VDMOSFET.

© 2016 Elsevier Ltd. All rights reserved.

1. Introduction

Silicon carbide VDMOSFETs have attracted more attentions due to their many inherent advantages, such as high operational temperature, high switching speed, and normally-off operation property and more simplified gate drive circuits, over other types of switch devices applied in low or medium power fields [1–5]. It can be widely used in hybrid electric vehicles, Photovoltaic (PV) inverters, power supplies Uninterruptible Power Supply (UPS), industrial motor drives, traction, and wind turbine controls, and so on [6–8]. Since the first high-voltage vertical double implanted power MOSFET (VDMOSFET) was reported by Shenoy et al. on 6H-SiC in 1997 [9], great progress in 4H-SiC VDMOSFETs has been achieved recently [10–13].

In order to realize higher breakdown voltage for 4H-SiC VDMOSFETs, the design of edge termination is the critical issue, several edge termination structures can be used for 4H-SiC VDMOSFETs [14,15], such as field limiting ring (FLRs) and junction

termination extension (JTE) [15,16]. Compared with FLRs termination, JTE termination requires additional implantation process and its blocking characteristic is sensitive to the doping concentration of JTE region, which limits its practical application in 4H-SiC VDMOSFETs. Therefore, the FLRs termination is the first choice for 4H-SiC VDMOSFETs, because it can be formed together with other regions of VDMOSFETs in the same implantation process, simplifying the fabrication procedure. Traditional FLRs in 4H-SiC VDMOSFETs are formed by heavily doped P⁺ region which is used for ohmic contact with P-well [17,18], but the blocking characteristics and stability of device are influenced by the surface damage of wafer caused by high dose and energy Al ion implantations, in which a higher density of interface traps induced by ion implantation in the P⁺ FLRs termination will affect the characteristics of SiC power devices with FLRs [20]. Furthermore, the low activation rate of the high concentration of implanted ions will increase the process difficulty and cost.

In this paper, 4H-SiC VDMOSFETs with the lightly doped P-well FLRs have been successfully fabricated on 10 μm thick 4H-SiC N-type epi-layer, and the breakdown voltage (BV) of 1610 V is yielded with about 90% value of the plane parallel breakdown voltage.

* Corresponding author at: Key Laboratory of Wide Band Gap Semiconductor Technology, Xidian University, Xi'an 710071, China.

E-mail address: xytang@mail.xidian.edu.cn (X.Y. Tang).

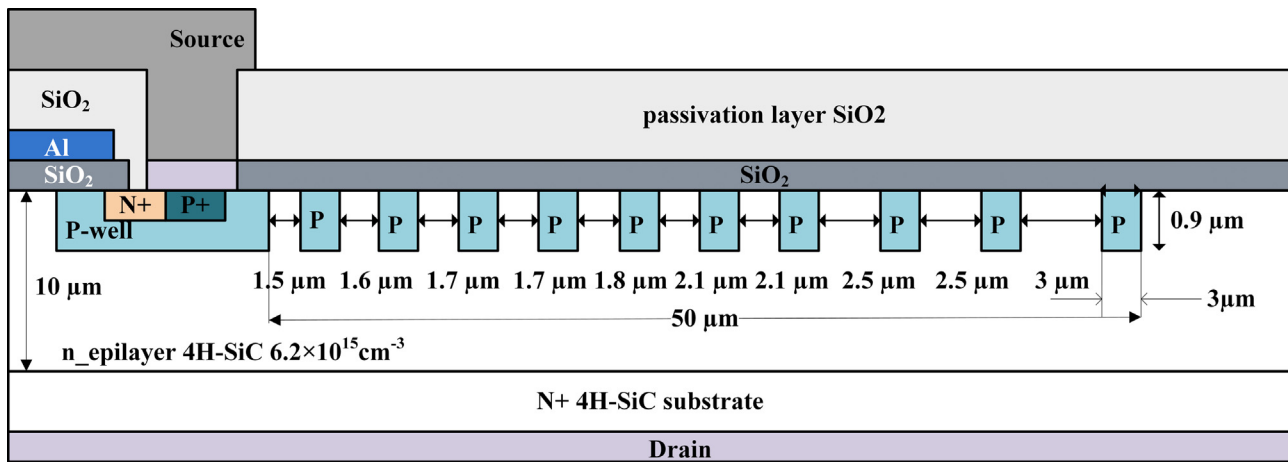
2. Termination design

The termination design of 4H-SiC VDMOSFET is made when the specifics and structure of 4H-SiC VDMOSFET are fixed. Fig. 1 shows the schematic structure of 4H-SiC VDMOSFET, which consists of vertical double-implanted MOSFET and a number of termination FLRs. In Fig. 1(a), the lightly doped FLRs termination is formed at the same time with P-well ion implantation, named P-well FLRs, and Fig. 1(b) illustrates the traditional heavily doped FLRs termination, formed at the same time with P⁺ region, named P⁺ FLRs. As can be shown from Fig. 1(a), P-well acts as either the active region of 4H-SiC VDMOSFET or termination ring. Therefore, P-well design is a critical issue for high performance of 4H-SiC VDMOSFET with efficient termination.

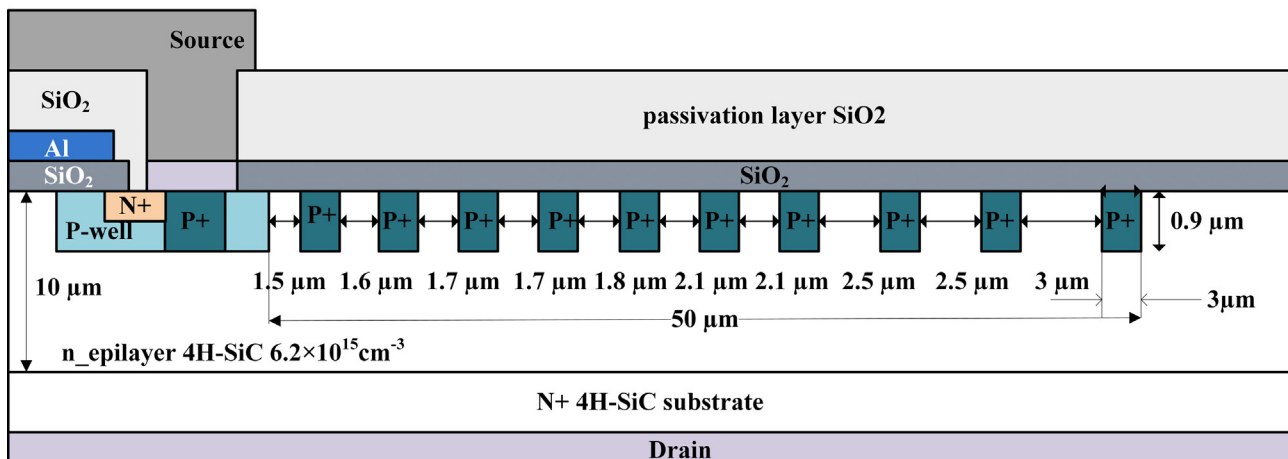
In the P-wells design, there are several basic factors involved. The punch-through effect between the N⁺/P-well/N[−] has to be considered to ensure the breakdown voltage of device, which is correlated with the ion implanted depth and doping concentration distribution of the P-well, and the surface concentration of P-well also affects threshold voltage value of VDMOSFET. In addition, the surface damage induced by ion implantation will lower the surface mobility of the device because multi ion implantation is required for deep depth of P-well so that the implantation energy and dose should be carefully designed for decreasing the effects of ion implantation on surface mobility. Based on above issues, the

suitable P-well implantation parameters have been designed. The profiles of P-well Al ion implantation simulated by TRIM are shown in Fig. 2, using multi ion implantation with the energy of 80 keV, 200 keV and 350 keV and the dose of $4 \times 10^{12}/\text{cm}^2$, $2.87 \times 10^{13}/\text{cm}^2$ and $9.52 \times 10^{13}/\text{cm}^2$, respectively. The doping profile of the P-well meets the demands, including the threshold voltage of 5.5 V without taking interface charges into account and punch-through voltage to be much larger than breakdown voltage. For the traditional termination design, the depth of P⁺ region should be larger than P-well in P⁺ FLRs termination to protect the edge corner of P-well. Meanwhile, the surface concentration of P⁺ region should be high enough to ensure the formation of p-type ohmic contact. Doping profile of P⁺ FLRs in Fig. 1(b) is also shown in Fig. 2.

Performance of the 4H-SiC DMOSFET has been simulated by 2-D device simulation tool DESSIS-ISE. The basic physical models for 4H-SiC, such as Bandgap energy [21], effective mass for electrons and holes [22], and incomplete ionization of impurities, are used in simulations. The ionization coefficients model proposed by Okuto and Crowell [23] is used in this work. In this paper, the breakdown voltage is defined as the voltage at which the current increases rapidly. The FLRs termination structure with non-linearly variable ring spacing is adopted. Compared with FLRs termination with constant spacing, it can achieve higher termination efficiency with same termination area [24]. In FLRs termination, the breakdown voltage is sensitive to the first guard spacing (d_1).



(a)



(b)

Fig. 1. Schematic structure of 4H-SiC VDMOSFET with (a) P-well FLRs termination and (b) P⁺ FLRs termination.

Download English Version:

<https://daneshyari.com/en/article/5010392>

Download Persian Version:

<https://daneshyari.com/article/5010392>

[Daneshyari.com](https://daneshyari.com)