Solid-State Electronics xxx (2016) xxx–xxx

Contents lists available at ScienceDirect

Solid-State Electronics

journal homepage: www.elsevier.com/locate/sse

Characterization of high-dose and high-energy implanted gate and source diode and analysis of lateral spreading of *p* gate profile in high voltage SiC static induction transistors

Hidekatsu Onose [a,*], Yutaka Kobayashi [b], Jin Onuki [c]

[a] Hitachi, Ltd., Center for Technology Innovation – Electronics, Research & Development Group, Energy Conversion Electronics Research Department, 1-280, Higashi-Koigakubo, Kokubunji-shi, Tokyo 185-8601, Japan
[b] Material Science & Engineering, College of Engineering, Ibaraki University, 12-1, Nakanarusawa-cho 4-chome, Hitachi-shi, Ibaraki-ken 316-851, Japan
[c] Graduate School of Science and Engineering, Ibaraki University, 4-12-1, Nakanarusawa-cho, Hitachi-shi, Ibaraki-ken 316-8511, Japan

ARTICLE INFO

Article history:
Received 20 June 2016
Received in revised form 28 October 2016
Accepted 4 November 2016
Available online xxxx

The review of this paper was arranged by Prof. S. Cristoloveanu

Keywords:
SiC
SIT
Diode
Implantation
Defect
Lateral spreading

ABSTRACT

The effect of the *p* gate dose on the characteristics of the gate-source diode in SiC static induction transistors (SIT) was investigated. It was found that a dose of 1.5×10^{14} cm^{-2} yields a *pn* junction breakdown voltage higher than 60 V and good forward characteristics. A normally on SiC SIT was fabricated and demonstrated. A blocking voltage higher than 2.0 kV at a gate-source voltage of −50 V and on-resistance of 70 mΩ cm^2 were obtained. Device simulations were performed to investigate the effect of the lateral spreading. By comparing the measured *I-V* curves with simulation results, the lateral spreading factor was estimated to be about 0.5. The lateral spreading detrimentally affected the electrical properties of the SIT made using implantations at energies higher than 1 MeV.

1. Introduction

The electrical properties and current ratings of silicon carbide (SiC) power devices are evolving in accordance with the goals of reducing loss, improving efficiency, and reducing the size of systems. In particular, SiC Schottky barrier diodes with blocking voltages of 600 V or 1200 V are now being marketed as discrete diodes or power modules in combination with Si insulated-gate bipolar transistors (IGBTs) [1–3].

Similar to diodes, a static induction transistor (SIT) or a junction field effect transistor (JFET) has no interface between SiC and SiO_2 in the channel region [4–8]. Although a SIT has no interface-related reliability problem, normally on operation, in which a negative gate-source voltage is used to reach the off-state, has so far prevented its use on a large scale. Recently, a cascode circuit switch combining a high-voltage SiC SIT and low-voltage Si MOSFET has been proposed as a solution to this problem [9]. Even if the SiC SIT is of the normally on type, the cascode switch can be operated as a normally off mode switch because a negative voltage between the SIT gate and SIT source is applied by the cascode connection at the gate terminal voltage of 0 V.

In Si SITs, an n^+ source is formed in the n^- area to create a high reverse gate-source voltage. On the other hand, the n^+ source can directly contact the *p* gate in SiC-SIT. Iwasaki et al. proposed a novel structure in which the edges of the n^+ source overlap the *p* gate [10]. Fig. 1 shows a schematic cross section of this SiC-SIT. The channel width W_{ch} is determined automatically by the gate implantation in this structure. The n^+ source is wider than the channel; as a result, a narrower channel can be formed without any restriction on the alignment between the n^+ source and the *p* gate and larger ratios of the blocking voltage and the reverse gate voltage, which is called the blocking gain, can be expected as a result. We have fabricated such SiC-SITs and presented their characteristics [11,12].

In the above papers, the channel width was selected such that a blocking voltage higher than 2.0 kV would be obtained and the results for the on-resistance were discussed. An effective index that characterizes normally on SITs is the blocking gain, which is

* Corresponding author at: Hitachi Power Semiconductor Device, Ltd., Product Division 1, 2-2 Omika-cho 5-chome, Hitachi-shi, Ibaraki-ken 319-1221, Japan.
E-mail address: Hidekatsu.onose.cs@hitachi.com (H. Onose).

http://dx.doi.org/10.1016/j.sse.2016.11.004
0038-1101/

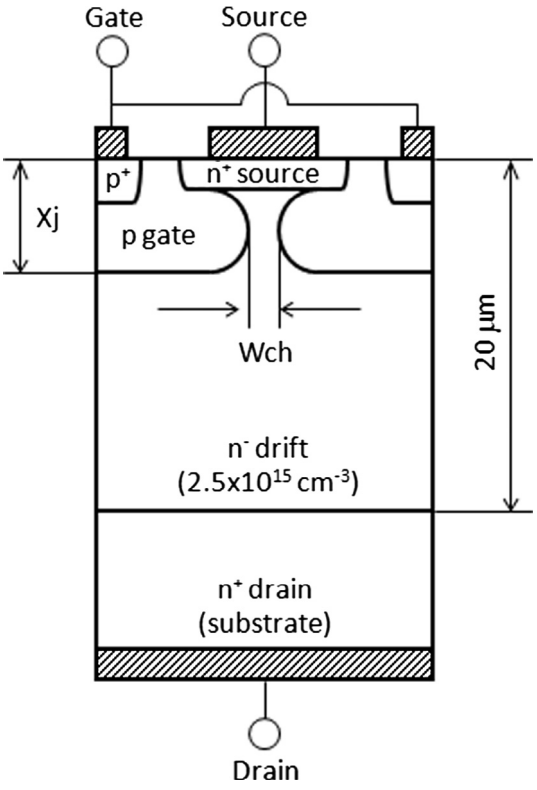

Fig. 1. Schematic cross sections of the vertical SIT. The n^+ source and p gate overlap.

defined as the ratio between the blocking voltage and reverse gate voltage in the off-state. To facilitate a gate drive, a high blocking gain would be advantageous. With this goal in mind, the pn diode between the n^+ source and the p gate and lateral spreading of the p gate should be characterized.

This paper examines the characteristics of the junction between the n^+ source and p gate in detail and discusses the relationship between the characteristics of SiC SITs and lateral spreading.

2. Dose conditions of *p* gate and electrical properties of fabricated SITs

Fig. 2 shows an outline of the implantation process used to fabricate the SIT. The n^+ drain layer was a 4H SiC substrate. The drift layer was an epitaxial layer whose thickness and concentration were 20 μm and 2.5×10^{15} cm^{-3}. The p gate was formed using high-energy aluminum implantations at 1100 keV and 1300 keV to achieve a channel deeper than 1.0 μm. No other aluminum implantations were used to form the p gate. A CVD-SiO_2 layer was used as an implantation mask, because the implantation energies were higher than 1 MeV. The total dose condition of the p gate was used as a parameter. The electrical properties of 1.5×10^{14} cm^{-2} and 1.5×10^{15} cm^{-2} doses were compared. The contact p^+ region was formed with multiple aluminum implantations from 25 keV to 450 keV. The n^+ source was formed with multiple nitrogen implantations from 30 keV to 180 keV. The surface concentration and the depth of the n^+ source are 1×10^{20} cm^{-3} and 0.45 μm. The width of the mask for the n^+ source was 8 μm, while that for the channel for the p gate ion implantation was 3 μm. Since the n^+ source was sufficiently wider than the channel width, a source-gate overlapped structure could be formed. After the implantations, annealing at 1600 °C in argon repaired the lattice damage and activated the implanted atoms. Since the activation ratio of aluminum is from 40% after a 1600 °C anneal, the

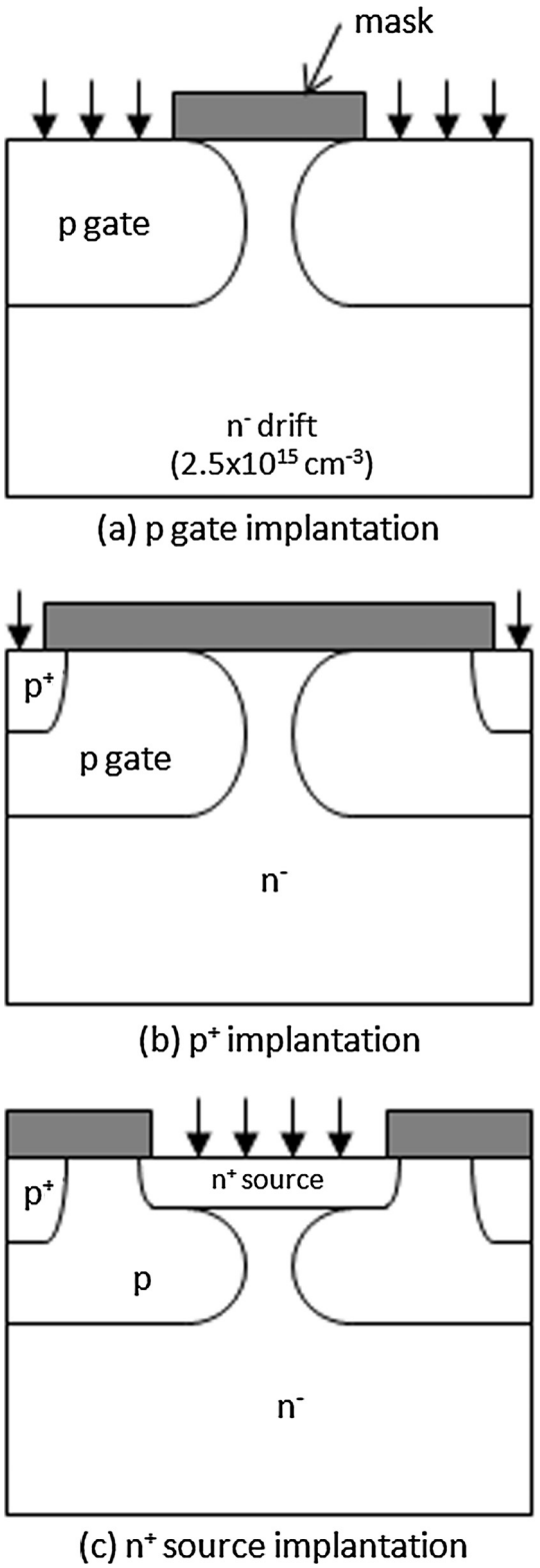

Fig. 2. Outline of the implantation process.

junction depth of the p gate was estimated to be 1.5 μm in the case of the 1.5×10^{15} cm^{-2} dose [13–16]. A thermal oxidation layer was formed in order to passivate the surface. Nickel was evaporated and sintered for the source, gate, and drain electrodes. The Ni electrodes were etched in a wet process. The space between the gate and source electrode was set to 6 μm for complete separation.

Please cite this article in press as: Onose H et al. Characterization of high-dose and high-energy implanted gate and source diode and analysis of lateral spreading of p gate profile in high voltage SiC static induction transistors. Solid State Electron (2016), http://dx.doi.org/10.1016/j.sse.2016.11.004