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A high aspect ratio silicon-fin FinFET fabricated upon SOI wafer

Yue-Gie Liaw [a], Wen-Shiang Liao [b,c,*], Mu-Chun Wang [d,*], Cheng-Li Lin [e], Bin Zhou [b], Haoshuang Gu [b], Deshi Li [c], Xuecheng Zou [a,*]

[a] Department of Electronic Science and Technology, Huazhong University of Science and Technology, Wuhan 430074, PR China
[b] Faculty of Physics and Electronic Technology, Hubei University, Wuhan 430062, PR China
[c] Faculty of School of Electronic Information, Wuhan University, Wuhan 430072, PR China
[d] Department of Electronic Engineering, Minghsin University of Science and Technology, Hsinchu 30401, Taiwan
[e] Department of Electronic Engineering, Feng Chia University, Taichung 40742, Taiwan

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ABSTRACT

Three dimensional (3-D) FinFET devices with an ultra-high Si-fin aspect ratio (Height/Width = 82.9 nm/8.6 nm) have been developed after integrating a 14 Å nitrided gate oxide upon the silicon on insulator (SOI) wafers through an advanced CMOS logic platform. The drive current (I_{ON}), off current (I_{OFF}), subthreshold swing (SS), drain-induced barrier lowering (DIBL) and transistor gate delay of 30 nm gate length (L_g) of FinFETs illustrate the promising device performance. The TCAD simulations demonstrate that both threshold voltage (V_{th}) and off current can be adjusted appropriately through the full silicidation (FUSI) of $CoSi_2$ gate engineering. Moreover, the drive currents of n- and p-channel FinFETs are able to be further enhanced once applying the raised Source/Drain (S/D) approach technology for reducing the S/D resistance drastically.

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1. Introduction

Seeking the high speed, low cost and high-volume capacity in IC chips is the development trend in the modern semiconductor industry [1,2]. As the process technology entering the nano-node generation, the FinFET structures are one of the bright stars in the tremendous competitive devices. In order to achieve an ultra-high density MOSFET-like IC product, a 3D FinFET device has emerged as a promising candidate as compared to other double gate device structures [3,4] due to its process compatibility with traditional logic devices. Moreover, FinFET devices present the advantages of avoiding shallow trench isolation process as well as effective improvement of I_{ON}, I_{OFF}, subthreshold swing, DIBL, and short channel effect owing to the good controllability of gate electrode surrounding the erected silicon body of Si-fin [5,6]. Besides the substrate with silicon bulk substrate [7,8], the device fabricated by using the silicon-on-insulator (SOI) wafer in high-performance computing (HPC) products is a suitable choice [9–11]. In this work, we report 3-D SOI FinFETs [12,13] with an ultra-high aspect ratio up to Si-fin Height/Width (H_{fin}/W_{fin}) = 82.9 nm/8.6 nm with promising performance such as I_{ON}, I_{OFF}, subthreshold swing (SS), and DIBL. We hereby focus on the gate dielectric with oxy-nitride (SiON) providing the higher k-value as compared with the pure gate oxide and preventing the implanted boron from penetrating gate electrode to N-well, not high-k dielectric (HK) like Hf-based dielectric (HfO_2 or $HfZrO_x$) [14,15] due to feasibly exposing the achievement of high aspect ratio Si-fin device and probably avoiding the interrupt of bonding between high-k dielectric and channel surface causing some unpredictable interfacial issues [16,17].

* Corresponding authors at: Faculty of Physics and Electronic Technology, Hubei University, Wuhan 430062, PR China (W.-S. Liao).

E-mail addresses: wsliaoumc@yahoo.com.tw (W.-S. Liao), mucwang@must.edu.tw (M.-C. Wang), estxczou@hust.edu.cn (X. Zou).

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2. Fabrication of FinFET devices

The SOITEC SOI wafers were applied to fabricate high-aspect ratio 3-D FinFETs with a conventional ULSI sub-65 nm generation logic technology [18,19]. Fig. 1 depicts a tilted sketch of this 3-D FinFET structure showing a poly-Si gate (red) lying across a Si-fin body (water blue) upon an SOI substrate with its drive-on currents passing through the two sidewalls of thin Si-fin body. In order to form this fin structure, the SOI crystalline silicon (*c*-Si) layer was thinned down with oxidation-and-etch process steps and the final *c*-Si thickness was controlled up to 80–90 nm. Furthermore, a furnace silicon oxidation processing was rendered to obtain an appropriate oxide layer for the subsequent Si-fin photolithography definition and plasma etching to achieve a desirable multiple Si-fin width such as 8.6–11.4 nm, as shown in Fig. 2. Continuously, a sacrificial thin oxide was grown upon both sides of the vertical sidewall to serve as a screen oxide and to remove the plasma etch damaged layer near the Si-fin surface. Subsequently, in order to gain more uniformly distributed implanted dopant profiles, boron (B) and arsenic (As) ions based on the TCAD simulation results with a 45° tilted implantation angle were employed for the threshold voltage (V_{th}) adjustment of n- and p-channel FinFETs.

After the 45°-tilted ion implantation for the threshold voltage tuning, the screening oxide was removed followed by the growth of a 14 Å (physical thickness) plasma nitrided oxide as the gate dielectric layer and an un-doped polysilicon (poly-Si) gate layer was deposited by low temperature chemical vapor deposition (LTCVD). Moreover, the high phosphorus (P) dosage implantation was applied for the reduction of n-channel poly-Si gate resistance and the high boron (B or BF_x) dosage was for p-channel gate resistance [20]. Due to the consideration obtaining a poly-Si gate length of 30 nm, an oxide hard mask and a 193 nm scanner were adopted. P-channel S/D extension (SDE) implantation [21,22] was skipped to avoid the excess boron diffusion in this work. Fig. 3 shows the tilt-SEM image of a multiple Si-fin SOI FinFET after the formation of poly-Si gate electrode.

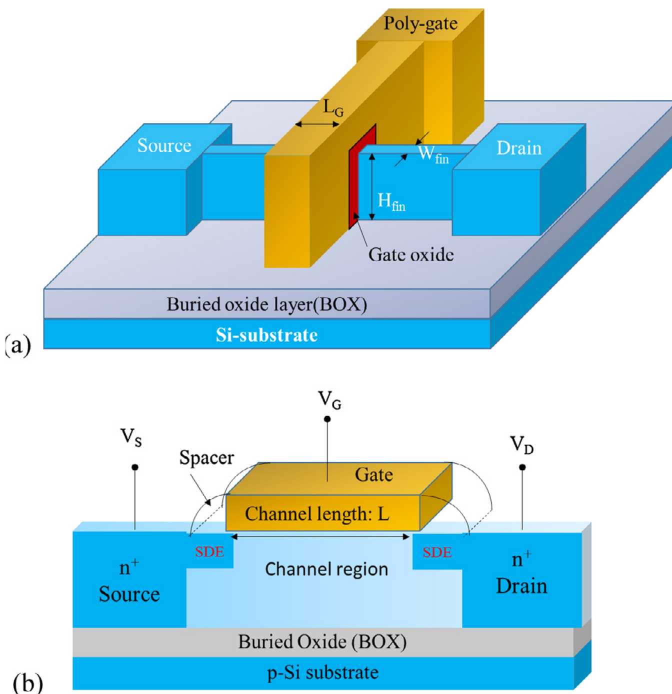

Fig. 1. Schematic contours of single n-channel FinFET: (a) 3-D top-view profile and (b) cross-sectional profile with S/D view on SOI substrate.

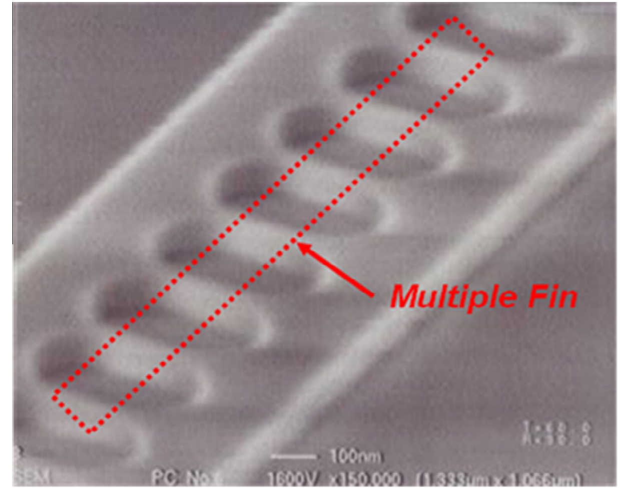

Fig. 2. The tilt-SEM image of a multiple Si-Fin with its Si-fin width (W_{fin}) of 17 nm.

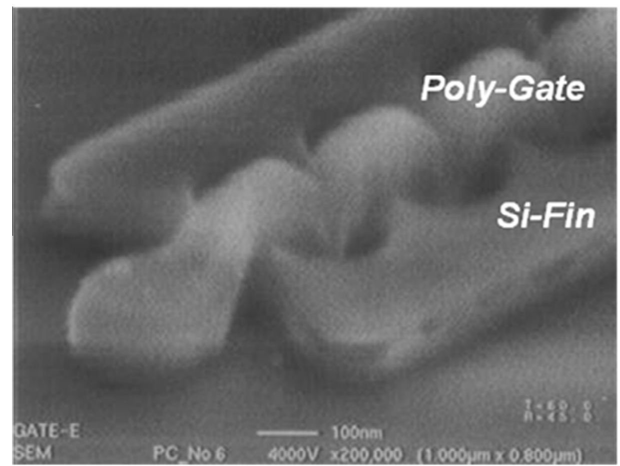

Fig. 3. The tilt-SEM image of a multiple FinFET after its poly-Si gate defined by photolithography, plasma etched and photoresist removed out.

Shortly thereafter, after the gate spacer formation both n^+ (As) and p^+ (B) source/drain ion implantations were conducted. A cobalt fully silicidation (FUSI) process for the poly-Si gate was also used followed by a standard copper interconnect process. Ultimately, a passivation of PECVD-SiO_x and SiN_x composite layer was deposited followed by the formation of aluminum bonding pads. The simple process flow in FinFET fabrication is illustrated in Fig. 4.

3. Results and discussion

In terms of basic electric characterizations of FinFET, they still follow the general formulas of 2-D MOSFET [23] although it provides the greater 3-D controllability in device channel, as given below.

$$I_{ON} = I_{ds_sat} = \frac{W}{2L} \cdot \mu_n \cdot C_{ox} \cdot (V_{gs} - V_{th})^2 \cdot (1 + \lambda \cdot V_{ds}) \quad (1)$$

$$V_{th} = \phi_{ms} - \frac{Q_f}{C_{ox}} - \frac{Q_d}{C_{ox}} + 2\phi_F \quad (2)$$

$$SS = 1000 \cdot \left(\frac{d\log(I_{ds})}{dV_{gs}}\right)^{-1} = 2.3\frac{kT}{q}\left(1 + \frac{C_d + C_{it}}{C_{ox}}\right) \quad (3)$$

where W: channel width, L: channel length, μ_n: channel mobility for n-channel device, C_{ox}: gate capacitance per area, λ: channel

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