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A compact model and direct parameters extraction techniques For amorphous gallium-indium-zinc-oxide thin film transistors

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ABSTRACT

An advanced compact and analytical drain current model for the amorphous gallium indium zinc oxide (GIZO) thin film transistors (TFTs) is proposed. Its output saturation behavior is improved by introducing a new asymptotic function. All model parameters were extracted using an adapted version of the Universal Method and Extraction Procedure (UMEM) applied for the first time for GIZO devices in a simple and direct form. We demonstrate the correct behavior of the model for negative V_{DS}, a necessity for a complete compact model. In this way we prove the symmetry of source and drain electrodes and extend the range of applications to both signs of V_{DS}.

The model, in Verilog-A code, is implemented in Electronic Design Automation (EDA) tools, such as Smart Spice, and compared with measurements of TFTs. It describes accurately the experimental characteristics in the whole range of GIZO TFTs operation, making the model suitable for the design of circuits using these types of devices.

1. Introduction

Transparent amorphous oxide semiconductor (AOS) materials have become of great interest for electronic device applications, i.e. thin film transistors (TFTs), electronic papers, sensors, etc., due to their promising characteristics such as large electron mobility, low temperature process, large area fabrication, low cost, and compatibility with flexible electronics [1,2]. Specifically, AOS TFTs have several features that make them attractive for applications in flexible flat-panel displays and large-area integrated circuits [3]. Among these, Ga–In–Zn–O (GIZO) TFTs have resulted very promising for switching devices in high-resolution active matrix liquid crystal displays (AMLCDs) with high frame rate and for current-driving devices in large-size active-matrix organic light-emitting diode (AMOLED) displays due to their high field-effect mobility, low off current, and excellent short-range uniformity [3–6]. Nevertheless, it is well known that, to obtain efficient circuits based on any device, preliminary modeling for circuit simulation is necessary.

In the last years, both numerical and analytical compact models for GIZO TFTs have been proposed. Even though several numerical models have been presented [7–11] they were not time efficient and so, not suitable for circuit simulation. Empirical models based on artificial neural networks (ANNs) were also demonstrated for this transistor technology, enabling accurate and continuous models but having parameters lacking explicit physical meaning [12].

On the other hand, compact models [13–15] are focused on the accurate physical-based description of the transistor's characteristics. Different methods are implemented to develop an analytical current-voltage model. In [14] is presented a GIZO current model based on MOSFET equations. Also, the surface potential based models, like [16] are not efficient for large display circuits design.

However, since AOS TFTs are based on a TFT structure similar to a-Si TFTs and the active layer is also amorphous, it seems that their behavior should be closer to that of a-Si:H TFTs [17–19]. On the other hand no direct parameter extraction methods have been presented for amorphous GIZO TFTs.

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Here we present an advanced compact model for AOS TFTs valid for GIZO devices and based on the physical behavior of the device, with an adequate consideration of its Density of States (DOS).

Our model is based on the unified model and extraction method (UMEM), which has been validated with devices made of different materials [17,20,21] and is applied for the first time to GIZO devices. The parameters are easily extracted from the experimental measurements with no need of using optimization methods. The model will include an improved asymptotic function for the saturation behavior [22] and an extended range of applications due to its proven symmetry of source and drain electrodes.

We implemented the GIZO model's Verilog-A code in Smart Spice and it is shown that a good agreement is obtained with experimental data. The presented model also, displays a smooth transition between the different regimes of operation of the TFT.

2. Experimental device

The GIZO TFTs on Si/SiO_2 substrates were fabricated and characterized at the Universidade Nova de Lisboa (UNL). Fig. 1(a) shows the schematic structure of the device with channel width W = 160 μm and channel length L = 20 μm, while the real GIZO TFT is shown in Fig. 1(b) [23].

The TFTs used in this work are fabricated with a staggered bottom gate top-contact structure, on a 5 layer process (gate electrode, dielectric, oxide semiconductor, source/drain electrodes, passivation).

All the layers except passivation (which is spin-coated SU-8) are produced by sputtering without intentional substrate heating, being patterned using conventional photolithography. Devices are annealed at 150 °C on a hot plate, for 1 h. Other processing details for the active layer an electrodes of the TFTs were previously reported elsewhere [24,25].

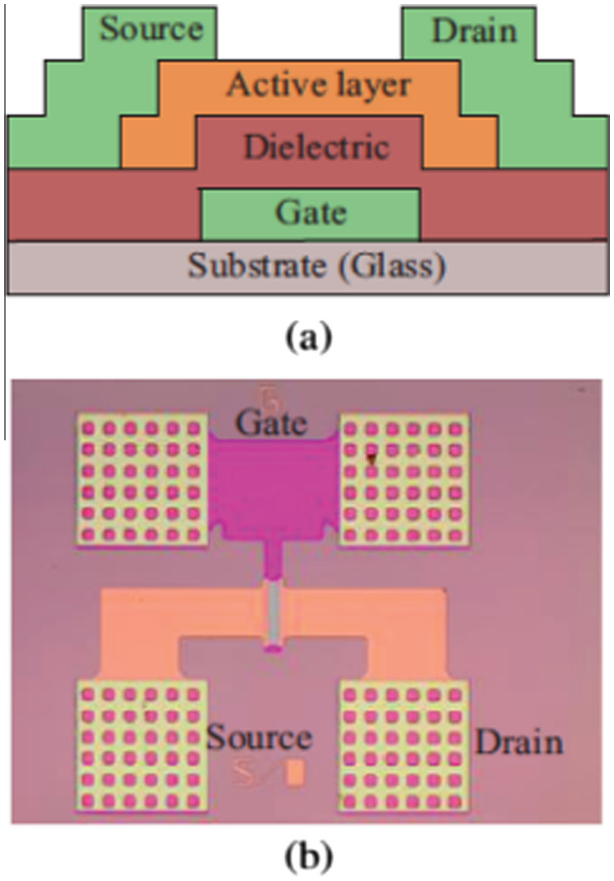

Fig. 1. (a) a-GIZO TFT structure, and (b) Fabricated device with W = 160 μm. L = 20 μm [23].

Static electrical characterization measurements were was performed with a probe station (Janis ST500) and a semiconductor parameter analyzer (Keithley 4200 SCS), in the dark, at room temperature, and in air atmosphere [26].

3. TFT modeling

The distribution of acceptor-type localized states in the mobility band of an amorphous n-type inorganic TFT is represented as the sum of the tail and deep states, which are exponentially dependent on the energy:

$$g_a = g_{ato} exp\left(-\frac{E_C - E}{kT_1}\right) + g_{ado} exp\left(-\frac{E_C - E}{kT_2}\right) \quad (1)$$

where g_{ato} and g_{ado} are the tail and deep acceptor densities extrapolated at $E = E_C$ and E_C is the conduction band energy; T_1 and T_2 are the characteristic temperatures of the tail and deep states respectively and k is the Boltzmann constant.

3.1. Above threshold regime

Typically, in amorphous TFTs the field effect mobility above threshold ($V_{GS} > V_T$) is well represented by the power law equation [27,28]:

$$\mu_{FET} = \frac{\mu_0}{Vaa^{\gamma_a}}(V_{GS} - V_T)^{\gamma_a} \quad (2)$$

where V_T is the threshold voltage, V_{aa} and γ_a are parameters defining the variation of mobility with gate bias in the above threshold condition, and are extracted by UMEM according to [17]. μ_0 is used for dimensional purposes and is taken as 1 cm^2/Vs.

3.1.1. Output asymptotic behavior

The output conductance is usually modeled by multiplying the total current by $(1 + \lambda V_{DS})$ [28], where λ is the saturation coefficient. Its physical origin is related to the channel length modulation and defines the non-ideal output curve at high V_{DS}.

According to this standard procedure, the asymptotic current will be calculated as $I_{a1} = I_{sat}(1 + \lambda V_{DS})$, where I_{sat} is the current in saturation. The output asymptote I_{a1} defines a higher current than the actual one, which gradually tends to the asymptotic current as V_{DS} becomes sufficiently high.

The disadvantage of this approach is that the currents I_{a1} and the real I_{DS} are too far apart and in general this gives rise to an inaccurate prediction of the low-voltage output conductance [29].

In order to overcome this problem, a different multiplication factor is proposed [22] giving a new asymptotic current $I_{a2} = I_{sat}[1 + \lambda(V_{DS} - V_{sat})]$, where $V_{sat} = \alpha_s(V_{GS} - V_T)$ is the saturation voltage and α_s is the saturation parameter that defines the saturation voltage. In this case I_{a2} is closer to I_{DS}, so the fitting accuracy is incremented not only for the I_{DS} but also for the output conductance, which is an important parameter for analog circuit simulations.

This method [22], prevents unexpected overestimation of low V_{DS} conductance by reducing the contribution of the asymptotic term in the linear regime.

We also include the function V_{DSe} which only enables a smooth transition between linear and saturation regimes and it will be approximately equal to V_{DS} when $V_{DS} << V_{sat}$ and approximately equal to V_{sat} when $V_{DS} >> V_{sat}$.

$$V_{DSe} = V_{DS}\left[1 + \left|\frac{V_{DS}}{V_{sat}}\right|^m\right]^{-\frac{1}{m}} \quad (3)$$