Accepted Manuscript

Simulation-Based Study of Negative Capacitance Double-Gate Junctionless Transistors with Ferroelectric Gate Dielectric

Chunsheng Jiang, Renrong Liang, Jing Wang, Jun Xu

PII: S0038-1101(16)30128-9
DOI: http://dx.doi.org/10.1016/j.sse.2016.09.001
Reference: SSE 7076

To appear in: *Solid-State Electronics*

Received Date: 15 June 2016
Revised Date: 31 August 2016
Accepted Date: 7 September 2016

Please cite this article as: Jiang, C., Liang, R., Wang, J., Xu, J., Simulation-Based Study of Negative Capacitance Double-Gate Junctionless Transistors with Ferroelectric Gate Dielectric, *Solid-State Electronics* (2016), doi: http://dx.doi.org/10.1016/j.sse.2016.09.001

This is a PDF file of an unedited manuscript that has been accepted for publication. As a service to our customers we are providing this early version of the manuscript. The manuscript will undergo copyediting, typesetting, and review of the resulting proof before it is published in its final form. Please note that during the production process errors may be discovered which could affect the content, and all legal disclaimers that apply to the journal pertain.

ACCEPTED MANUSCRIPT

Simulation-Based Study of Negative Capacitance Double-Gate Junctionless Transistors with Ferroelectric Gate Dielectric

Chunsheng Jiang [a], Renrong Liang[a, *], Jing Wang [a], and Jun Xu[a]

[a]Tsinghua National Laboratory for Information Science and Technology, Institute of Microelectronics, Tsinghua University, Beijing 100084, China

[*]liangrr@tsinghua.edu.cn

Abstract

In this work, a kind of negative capacitance double-gate junctionless transistor (NC-DG-JLT) with ferroelectric (FE) gate dielectric and metal-ferroelectric-metal-insulator-semiconductor (MFMIS) structure is proposed. It is demonstrated that NC- DG-JLTs can lower off-state current, improve on-state drain current, and lower subthreshold swing at the same time compared with its conventional DG JLT counterpart using numerical simulation. The steeper subthreshold swing (*SS*<60 mV/dec) is achieved at room temperature. The related physical mechanisms are discussed in detail. The low off-state current and high on/off current ratio could be obtained even for ultra-small transistors by optimizing the device parameters. NC-DG-JLTs have a great potential for low power dissipation applications.

PACS: 02.60.Cb; 77.55.fp

Keywords: Junctionless transistor; ferroelectric gate dielectric; negative capacitance; power dissipation applications; numerical simulation

Download English Version:

https://daneshyari.com/en/article/5010421

Download Persian Version:

https://daneshyari.com/article/5010421

Daneshyari.com