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Impact of hydrogen anneal on low frequency noise of n- and p-MOSFET

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ABSTRACT

In this paper, we present a detailed investigation of the impact of hydrogen anneal on the low frequency noise spectra of n- and p-MOS devices from an advanced CMOS technology node. We investigate the impact of hydrogen anneal in three different wafers, one with one time hydrogen anneal step (1×H2), one with two times (2×H2) and one without hydrogen anneal (w/o H2). The results demonstrate that the carrier number with correlated mobility fluctuations model can explain accurately the 1/f noise results. A significant reduction of the 1/f noise level was observed for the device treated with two times hydrogen anneal.

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1. Introduction

Low-frequency noise (LFN) is considered as a non-destructive and powerful experimental tool to evaluate the quality of the dielectric interface [1,2], which is directly related to the quality of electronic devices. LFN can limit the performance of VCO, DRAMs, SRAM cells, inverters and others mixed signal circuits [3,4]. Therefore, it is essential to minimize the 1/f noise level to improve the performance of electronic circuits using advanced CMOS process integration concepts.

In MOSFETs, it is generally accepted that the flicker (1/f-like) noise originates either from carrier number fluctuations (CNF) (Eqs. (1) and (2) of Table 1) [4] or from Hooge mobility fluctuations [5]. The CNF noise is due to carrier exchange between the near-interface gate dielectric traps and the channel. The charge fluctuations in the gate dielectric could also induce fluctuations of the carrier mobility, giving rise to the so-called correlated mobility fluctuations (CMF) (Eqs. (3) and (4) of Table 1) [6–9].

Although the huge improvement of 1/f physical noise modelling there are still many things to be done in order to better understand and improve the low frequency noise in CMOS devices. In this work, it is demonstrated that the hydrogen anneal can be used in any standard CMOS process to improve the quality of the gate/oxide interface to lower the low frequency noise of n- and p-MOSFET by at least one decade. Here for the first time we investigated the impact of anneal steps at various process stages with and without H2 in a standard CMOS technology node on the low frequency noise behavior of n- and p-MOS devices. We investigated standard bulk planar CMOS MOSFET and the anneal steps carried out for ILD densification and contact liner in contrast to the work of [10]. In their work they investigated FINFET on SOI and they performed the hydrogen anneal in order to reduce the sidewall roughness and the etch damage.

2. Experiment

Electrical measurements were carried out on n- and p-MOS transistors issued from an advanced bulk CMOS technology node. The channel material is Si. The width and the length of the measured device was 5 and 0.18 μm, respectively. The gate stack consists of SiON-based oxide dielectric with equivalent oxide thickness of 4.6 nm. The different processed wafers didn't show any difference in EOT values. Table 2 shows the process sequence of an interlevel dielectric (ILD) stack of a conventional CMOS technology with the investigated process steps. The ILD is a conventional layer stack of Si_3N_4 barrier layer of 50 nm at the bottom and a BSPG layer of around 800 nm. The anneals were done in a vertical furnace in pure N2 or in forming gas (95% N2/5% H2) at 600 °C for 1 h in order to improve the barrier properties of the TiN liner and saturate the dangling bonds in the gate oxide interface.

Static characterization was performed in order to obtain the transfer (ID-VG) characteristics and then to extract typical MOSFET

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Table 1
CNF and CMF low frequency model.

$$\frac{SID}{ID^2} = \left(\frac{GM}{ID}\right)^2 \cdot SVFB \quad (1) \qquad SVFB = \frac{q^2 \cdot kT \cdot \lambda \cdot N_t}{W \cdot L \cdot C_{ox}^2 \cdot f^\gamma} \quad (2)$$

$$\sqrt{SVG} = \sqrt{SVFB} + \Omega \cdot \sqrt{SVFB} \cdot \frac{ID}{GM} \quad (3)$$

$$\frac{SID}{ID^2} = \left(\frac{GM}{ID}\right)^2 \cdot SVFB \cdot \left(1 + \Omega \cdot \frac{ID}{GM}\right)^2 \quad (4)$$

Where $\Omega = a_{sc} \cdot \mu_{eff} \cdot C_{ox}$, a_{sc} is the Coulomb scattering coefficient, μ_{eff} is the effective carrier mobility, C_{ox} is the gate dielectric capacitance per unit area, SVFB is the flat-band voltage spectral density, $SVG = f^\gamma \cdot SID/GM^2$ the input voltage spectral density, ID is the drain current, GM is the transconductance, SID is the drain current noise spectrum, kT is the thermal energy, λ is the tunnel attenuation distance (≈0.1 nm for SiO_2), q is the elementary charge, f is the frequency, γ is the slope of the drain current spectrum (close to 1) and N_t is the gate dielectric trap density in $cm^{-3}\ eV^{-1}$.

Table 2
Process flow.

Process flow	w/o H2	1×H2	2×H2
ILD deposition			
ILD densification	N2 anneal	N2 anneal	H2 anneal
CMP ILD Planarization			
Contact mask			
Contact etch			
Contact liner deposition			
Contact liner anneal	N2 anneal	H2 anneal	H2 anneal

parameters such as transconductance GM. LFN measurements where performed using a Cascade Edge system [11] for low frequency noise measurements. Drain current noise measurements were carried out in linear and saturation region of operation. The drain voltage VD was fixed to ±0.1 and ±1.8 V, respectively, for n- and p-MOS in linear and saturation and the gate voltage varied from weak to strong inversion. The experimental bandwidth is 1 Hz–1 kHz. It should be noted that all the spectra presented in this work are the average of at least 12 dies, thus suppressing the impact of RTS-induced Lorentzian-like spectra in small area devices [12]. All noise parameters were extracted at f = 10 Hz.

The analysis procedure is divided in three parts. First, we present the device static and LFN characteristics for each process split. Then, we investigate the model that can accurately explain the noise data. Finally, we present the comparison of LFN between the process splits and the impact of hydrogen anneal on noise level.

3. Results and discussion

Typical ID-VG and GM-VG characteristics illustrating the devices static functionality are shown in Figs. 1 and 2 for all process splits and drain biases n- and p-MOS, respectively. There is a small difference between the characteristics of the different

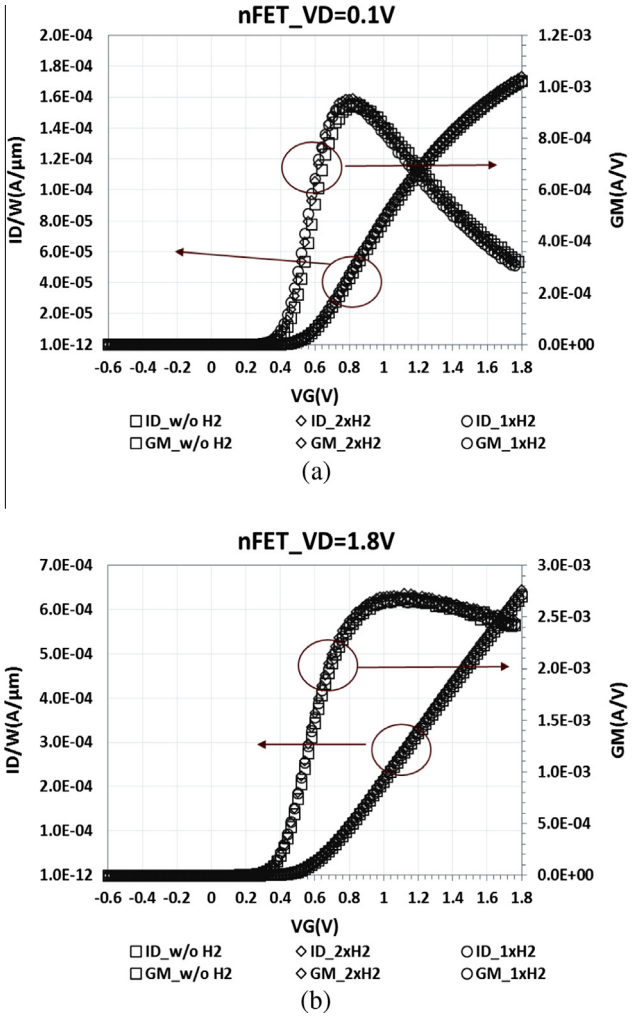

Fig. 1. ID/W-VG and GM-VG curves in log-lin axis for n-MOS in (a) linear and (b) saturation region of operation for all measured wafers, respectively.

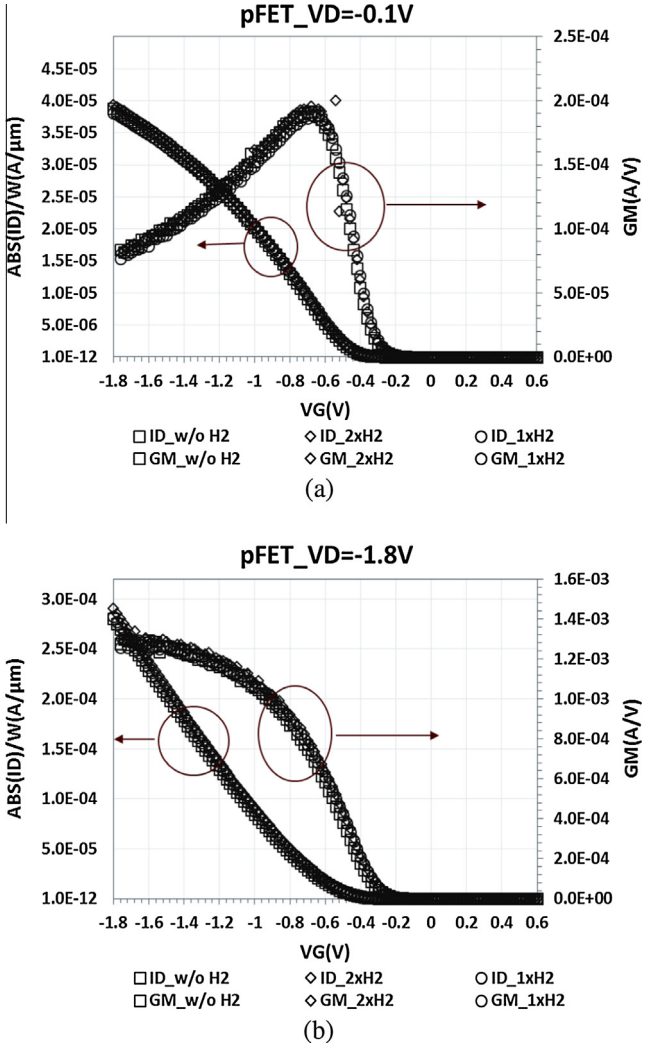

Fig. 2. ID/W-VG and GM-VG curves in log-lin axis for p-MOS in (a) linear and (b) saturation region of operation for all the measured wafers, respectively.

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