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The defect-centric perspective of device and circuit reliability—From gate oxide defects to circuits

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ABSTRACT

As-fabricated (time-zero) variability and mean device aging are nowadays routinely considered in circuit simulations and design. Time-dependent variability (reliability-related variability) is an emerging concern that needs to be considered in circuit design as well. This phenomenon in deeply scaled devices can be best understood within the so-called defect-centric picture in terms of an ensemble of individual defects. The properties of gate oxide defects are discussed. It is further shown how in particular the electrical properties can be used to construct time-dependent variability distributions and can be propagated up to transistor-level circuits.

1. Introduction

Variability of as-fabricated (i.e., time-zero) parameters of modern VLSI devices has been considered in circuit design tools for some time (Fig. 1a). With the exception of Time-Dependent Dielectric Breakdown (TDDB) [1,2], circuit lifetime estimation due to Field-Effect Transistor (FET) gate-oxide degradation (aging) mechanisms is presently based on projecting only the *mean* parameters shifts (Fig. 1b) [3]. The combination of both hitherto orthogonal efforts used in determining circuit operating margins is illustrated in Fig. 1c.

It has long been accepted that in mechanisms associated with FET *gate* current, such as Stress-Induced Leakage Current (SILC) and TDDB, only a handful of defects will cause significant current increases and can bridge the gate oxide, presently ~1 nm thick. Similarly, as lateral dimensions of VLSI devices are reduced toward the 10 nm range, just a few stochastically-behaving defects present in the FET gate oxide will have a sizable impact on the *drive* current as well. These phenomena result in additional, *time-dependent* variability in deeply-scaled devices, and their manifestation in the form of Random Telegraph Noise (RTN) has been extensively studied by many groups [4–13]. Here we build upon those observations and show how the same, physics-based considerations give rise to a new, *statistical* perception of other gate-oxide degradation mechanisms, such as Bias Temperature Instability (BTI) and Hot Carrier Injection (HCI) [14–16]. This paradigm shift is illustrated in Fig. 2.

Since only a handful of defects (cf. $N_T = 12$ in Fig. 2b) will be responsible for the time-dependent effects in each deeply-scaled device, we maintain that understanding of degradation mechanisms at the level of individual defects is essential for simulations of time-dependent variability in circuits. This notion is indeed the basis of the so-called *defect-centric* picture and is hierarchically illustrated in Fig. 3. After defining basic variability terms, we review the properties of individual defects and show how to propagate these properties to higher hierarchical levels. We formalize the statistical description of time-dependent distributions (Fig. 1e) into simple equations and point out the parallels with time-zero variability. To estimate the full device and circuit parameter distributions at the end of useful lifetime, time-zero and time-dependent statistics have to be combined, as illustrated

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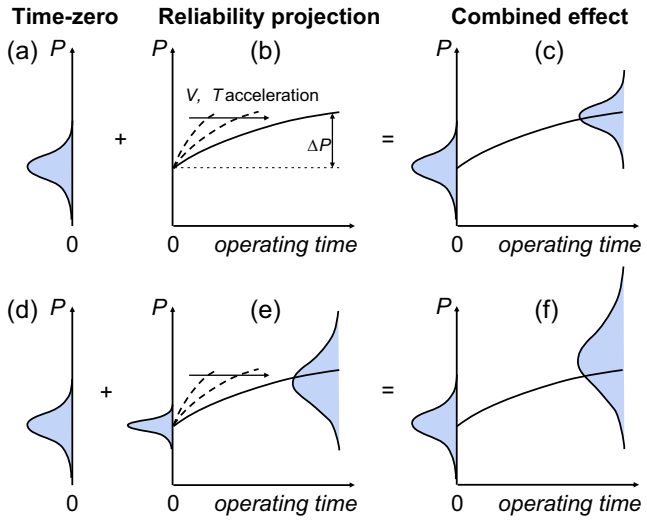

Fig. 1. A schematic representation of time-zero and time-dependent effects considered in circuit design. (a–c) Presently, time-zero variability of a device parameter P is considered together with the projection of the *mean* parameter shift ΔP (obtained by reliability engineers through bias and temperature accelerated tests) during aging. (d–f) Time-dependent variability is also considered, in contrast to (a–c).

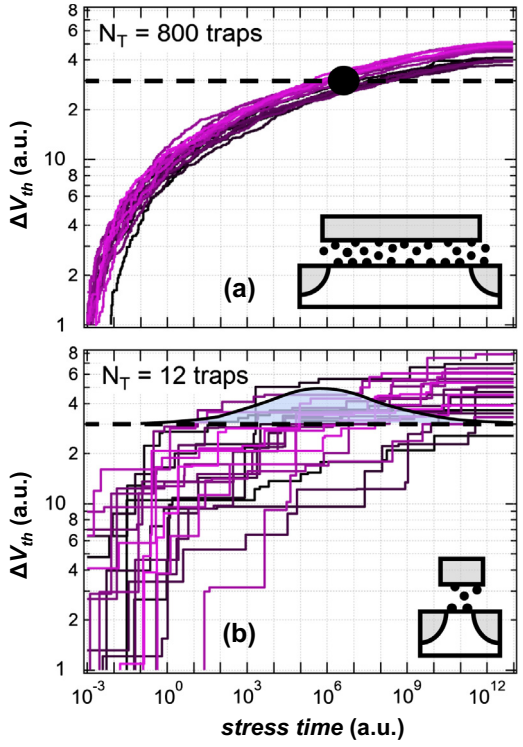

Fig. 2. (a) The random properties of many defects N_T in large devices average out, resulting in a well-defined lifetime while (b) the stochastic nature of a handful of defects in deeply-scaled devices becomes apparent, resulting in large variation in the lifetime. This also illustrates the paradigm shift in projecting reliability in deeply scaled devices (Fig. 1b and e) [17].

in Fig. 1d–f. Finally, we discuss how the combined variability can be propagated to and simulated at the circuit level.

2. Device variability

We refer to as-fabricated, *time-independent,* or *static,* device-to-device variability, as *time-zero* variability. *Time-dependent,* or *dynamic,* variability then refers to all variability due time-dependent effects. In this work, this is limited to effects due to defects (traps) present in FET gate dielectrics. The main emphasis of this Section is developing the time-dependent variability within the defect-centric picture. This is done Section 2.2. Subsections thereof then discuss the properties of individual traps (Section 2.2.1), both temporal and electric, the statistics of multiple traps (Section 2.2.2), and the experimental methods to characterize time-dependent variability (Section 2.2.3). The complete distribution (Section 2.3) is constructed from time-dependent variability and time-zero variability, discussed next.

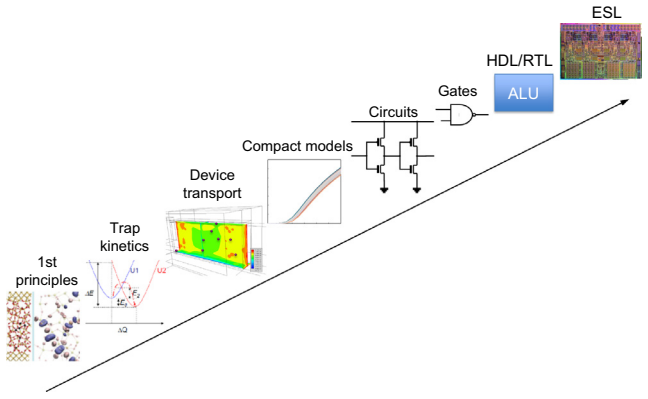

Fig. 3. Hierarchical levels of the defect-centric picture: Understanding of defect properties at the atomic level [18] can be propagated up to circuit design.

2.1. Time-zero variability

As-fabricated, i.e., time-zero variability, both systematic (process-induced) and random, is a well-known phenomenon in deeply-scaled VLSI technologies [19,20]. For example, the time-zero threshold voltages V_{th0} are assumed to be normally-distributed with mean $\langle V_{th0} \rangle$ and variance σ^2_{Vth0} [21]. Disregarding edge effects, the random component of σ^2_{Vth0} scales as

$$\sigma^2_{Vth0} \cong \frac{A^2_{Vth}}{A_G} \tag{1}$$

where A_{Vth} is a scaling factor and A_G the total channel area [22,23]. It should be noted that some variation-inducing effects, such as Line-Edge Roughness, will result in a departure from this ideal scaling rule in deeply scaled devices [24].

A large number of nominally identical devices need to be typically measured to establish A_{Vth}, while organization of devices into matched pairs or local arrays is used to separate the systematic and the random components [25].

2.2. Time-dependent variability

Similarly to time-zero variability, time-dependent variability also has random and systematic components [25–28]. Because of the limited number of gate-oxide defects N_T present in modern deeply downscaled FETs (e.g., $N_T = 10$ with defect density $10^{12}\,\mathrm{cm}^{-2}$ and $A_G = W \times L = 100 \times 10\,\mathrm{nm}^2$), other degradation mechanisms, such as RTN/BTI and HCI will be distributed as well [14,16,29]. Based on this simple fact we claim that *the time-dependent variability in deeply scaled devices can be best understood in terms of an ensemble of individual defects and their time, voltage, and temperature dependent properties.* This is indeed the underlying foundation of the defect-centric approach. To develop this approach further, we now discuss some of the relevant properties of individual defects.

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